CHAPTER 1

1.1 Motivation

The recurring demand and aggressive need for the low loss, high linearity, low power, low cost, reduced size and lightweight systems for defence, satellite and wireless applications leads to the search of an alternative technology to solid state devices [1]. These applications need more battery life with improved performance due to their strategic deployment. RF MEMS technology [2-4] is the one which has many current and future applications exacting these qualities include reconfigurable circuits, wireless systems for specific applications, wireless data links, switching networks, RF front end systems, Global positioning systems, phased array systems in radar and EW applications [5-9]. This technology also has the potential to enable wider operational bandwidths and eliminate off-chip passive components by the planar fabrication processes which are compatible with existing IC and MMIC processes for integration [10-12].

Phase Shifters are critical components in the Active/Passive Electronically steerable Antennas (AESA/PESA) for their applications in Missile Seekers, Radar and Electronic warfare systems. AESA/PESA offer many advantages over conventional mechanically scanned arrays such as fast scanning rate, light weight and beam shaping capability. More significantly, AESA/PESA eliminate the requirement of high power concentrated source as each radiating element is fed and controlled individually by the independent transmit-receive modules [13]. The electronic beam steering is best realized by using phase shifters to control the phase of the individual radiating element of the antenna array without any mechanical motion. The beam steering resolution is directly dependent on the number of bits of the phase shifter. Multi-bit phase shifters are used in phased array antennas to minimize the phase

quantization error. In general 3 or 4 bit phase shifters are employed in the commercial systems where as 5 or higher bit phase shifters are implemented in sophisticated military and aerospace applications to meet the high resolution and accuracy requirement [14]. Conventional phase shifters are developed using ferrite types, PIN diodes and MESFET. The ferrite phase shifter can handle high RF power but relatively consume large amount of DC power, expensive to fabricate and require manual tuning. Solid state phase shifters provide a good solution at microwave frequencies and have been used successfully in phased array applications but on contrary these incur high insertion loss leading to high gain requirement at microwave frequencies [15].

Ku band has wide range of applications in Defence and Space domain namely Airborne Radars, Missile Guidance, Collision Avoidance System, Battlefield Surveillance Radar, Missile Tracking and Telemetry as well as in satellite communication [16-18]. Moreover Ku band is a natural choice due its small size antenna and other system requirements. K_u band is also less vulnerable to rain fade than the K_a band frequency spectrum [19]. Practically the insertion loss of the solid state phase shifters in Ku band is of the order of 7-8 dB for 5-6 bit configurations [20]. *There is a need of high resolution, low insertion loss and low power consumption phase shifters in K_u band spectrum.* MEMS based device represent an extremely attractive alternative for the realization of programmable phase shifters.

RF MEMS Phase Shifters have shown their technical promise over the solid state type devices. RF MEMS phase shifters can be designed and developed with different topologies based on the application requirement. The implementation of the MEMS based Phase shifters leads to reduction in power consumption, size and weight which is very crucial for on-board defence and aerospace systems. Replacement by MEMS Phase Shifters even leads to reduction in RF gain requirement in transmit-receive (T/R) modules due to their very low

insertion loss[21-23] which results in elimination of an amplifier stage in the T/R chain. This further leads to reduction in dc power by20-100 mW per element across X to V band frequencies. It is substantial power reduction for space-based, airborne, and even low-power portable telecommunication and radar systems. This aspect becomes more significant as the number of elements in these applications ranges from few hundreds to thousands. MEMS have very low up-state capacitances and result in a wideband performance when compared to similar designs using solid state devices. The switching time of MEMS switches is of the order of 1-50 μs which allows them to be used in virtually all systems except fast airborne applications. The power-handling capabilities of MEMS devices are of the order of mW, which is sufficient for high frequency applications as they are placed before power amplifier in the T/R module. Typically observed millions cycle life time is enough for above mentioned application more specifically for on-board missile systems and single shot defence applications. Hence it is evident that RF MEMS phase shifters can be readily used in the above mentioned applications [24-25].

RF MEMS switch [26-27] is the integral part of the phase shifters and are needed in large numbers (typically 10-20), based on the configuration of the phase shifter. The performance of phase shifter solely depends upon the performance of switch. Electrical performance of solid-state switches degrades drastically beyond a few GHz [28-29]. On the other hand, the MEMS switches provide low insertion loss, high isolation, extremely high linearity and low power consumption over a much wider frequency range [30-31]. In addition non-linearties are non-existent in MEMS device as compared to semiconductor junctions in PIN diodes and GaAs FETs, except for the slight hysteresis noted on the CV characteristics of shunt switches. Their high integration levels and imperceptible inter modulations or harmonics further improve their overall performance. Therefore MEMS based switch are preferred over solid state based switch in reconfigurable and phased array antenna [32].The

switches can be designed to interface with 50 Ohm impedance across the broad range of frequencies when closed and nearly an open circuit when there is no connection. This property makes them an attractive choice for microwave applications.

The RF MEMS device development has been a challenge and is better understood during recent time. Numerous researchers have reported various analyses for long term operation of these devices. However there have been problems with regard to the stable operation of the RF MEMS devices. In spite of some active research in this area, *stable switching of signals is a problem which stems from the insufficient restoration force.* Also *there is lack of sufficient, consistent study in 5-bit phase shifter in Ku band*. These necessitate examining some new design with built-in reliability concept and process of these devices as well as development of 5-bit Ku band MEMS Phase Shifter.

1.2 Objectives of the thesis

The goal is to design & simulate, fabricate, characterize and optimize the RF MEMS switch and phase shifter for reconfigurable circuit and phased array applications respectively. Keeping the gaps in literature review, the following specific objectives are formulated for this thesis.

I. Design, simulation and Analysis of RF MEMS device i.e. switches for its performance and highlighting the challenges with built in reliability having low actuation potential.

II. Prototype fabrication, inspection and characterization of the capacitive and ohmic switches for a successful implementation in the Phase shifter circuits.

III. To Design, fabricate & demonstrate the development of the 5-bit RF MEMS based Phase Shifter in Ku band for implementation in Transmit-Receive Modules of Active Phased array application.

1.3 Thesis Outline

The thesis has been framed in nine chapters. First chapter discusses the motivation and objectives. The second chapter briefs the literature survey of the existing work. The third chapter summarizes the Design & Simulation of the shunt and ohmic RF MEMS switches. The fourth chapter contains the prototype fabrication, experimental set up, results & discussion of the RF MEMS switches on quartz. The fifth Chapter illustrates the Design & Simulation of the MEMS Phase Shifter configurations for Ku band. The sixth chapter deals with the Fabrication & Process Inspection of the phase shifter. The seventh chapter presents the On-Wafer RF Characterization of Single bits and 5 bit Phase Shifter. The eight chapter explains the control circuit and test jig development and the presents the results of microstrip Phase Shifter Characterization. Finally in chapter nine conclusion and plan for future work are outlined.

CHAPTER 2

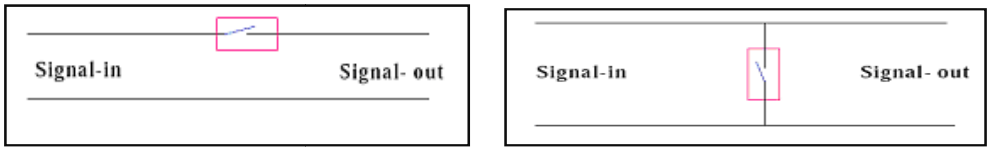
LITERATURE SURVEY

As described in the objective of the thesis, the aim of this work is to develop a 5 bit RF MEMS phase shifter in Ku band due to its application requirement in the Defence and Aerospace domain. The switch being an integral part of the phase shifter, the literature survey was focused on these two devices i.e. phase shifter and switch. This section describes the work carried out by the various researchers and their results. The gaps observed in the results are also discussed.

2.1 RF MEMS Switch – Brief Description and Fabrication

There are two basic design topologies namely shunt and series [33] switch used in RF to mm wave frequency. The ideal series switch results in an open circuit in the transmission line when no bias is applied called the up state. It results in a short circuit in the t-line when a bias voltage is applied. Ideal series switches have infinite isolation in the upstate and zero insertion loss in the down state position. The shunt switch is placed between transmission line and the ground depending upon the bias voltage; it either leaves the t-line unaffected or deflects it to ground. Therefore, the shunt switch [34] results in very low insertion loss when no bias is applied for up-state position and high isolation when bias is applied for down-state position. Shunt capacitive switches are more suited for higher frequencies in the GHz range. It is to be noted that both metal-metal and capacitive contact can be used in series and shunt configurations. However, it is preferred to use metal-metal contact switch in series

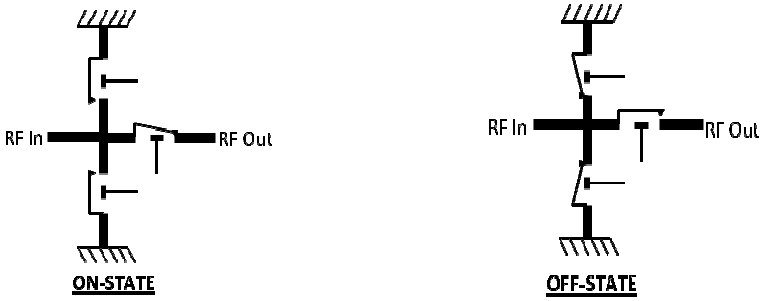
configuration and capacitive contact switch in shunt configuration. Simple illustrations are given below in Fig. 2.1 (a) for the series and (b) the shunt switch configurations.



(a) (b)

Fig. 2.1: (a) Series Switch - Output is "High" when switch is closed and (b) Shunt Switch - Output is "Low" when switch is closed.

The combined functioning of the switches is also illustrated by the sketches drawn in Fig. 2.2 (a) and (b) to achieve high isolation. Figure 2.2 (a) shows the on state whereas in the Fig. 2.2 (b) it is off as the states of the switches are just in opposite condition. The RF signal in the Fig. 2.2 (b) is grounded and high isolation can be achieved.



(a) (b)

Fig. 2.2: (a) and (b) Signal transmission flow of combined switches to achieve the high isolation.

Micromachining techniques have been evolved for MEMS fabrication [35]. These include the bulk and surface micromachining. In contrast to the bulk micromachining in which substrate material is removed by means of the physical or chemical means, the Surface micromachining builds microstructure by adding materials layer by layer on top of the substrate. In this process of adding and removing layers different structures are realized and interconnected using the multi mask fabrication process.

The use of bulk micromachining in fabrication of RF MEMS switches is very limited. Moreover it is very difficult to integrate the MEMS devices fabricated using this technique with IC components required for signal conditioning. Thus RF MEMS switches are almost exclusively fabricated using the surface micromachining technique [36]. The surface micromachining technique is best suited to integrate mechanical devices with integrated circuit (IC) components because this technique utilizes deposited thin films for fabrication of mechanical parts of the sensor. Figure 2.3 (a) and (b) shows the typical difference between the two techniques used for producing a micro cantilever beam [37-38].

Fig. 2.3: (a) Bulk micromachining (b) Surface micro machining.

As the processes for fabrication of the mechanical parts are similar to those for IC components with some additional steps, integration of MEMS and signal conditioning circuitry may be possible. As discussed in the previous section, fabrication of cantilevers or fixed-fixed beams is essential for realization of RF MEMS switches. The process can be modified for different materials for the beam, post and substrate. Also, some applications require complicated surface micromachining processes where many layers have to be deposited and selectively etched to realize the final structure. RF MEMS switch is one such application where typically five to eight masks may be needed to realize the full device. This is a multi-mask process device fabrication and selection of the sacrificial layer is very crucial. Many Researchers have used many materials as the sacrificial layer, out of these, photo resists [39-40] and polyimide [41] is very popular because these can be removed easily by

oxygen plasma [42] without affecting the membrane material. Hence selection of sacrificial layer has to be done keeping in view the process of removal.

2.1.1 RF MEMS Switch - Technology Development

Texas Instruments (now Raytheon) developed the first practical MEMS capacitive shunt switch Fig. 2.4 [43-44]. The switch is based on a fixed-fixed metal (Al or Au) beam design. The anchors are connected to the coplanar-waveguide ground plane, and the membrane is, therefore, grounded. In a microstrip implementation, the switch anchors are either connected to the ground plane using via holes or using a λ/4 radial stub. In the Raytheon design, a center pull-down electrode is used and a 1000-2000-Å silicon-nitride layer is used to isolate the metal membrane from the pull-down electrode. The actuation voltage was observed between 3-50V. The above mentioned studies do not cover the electromechanical analysis.

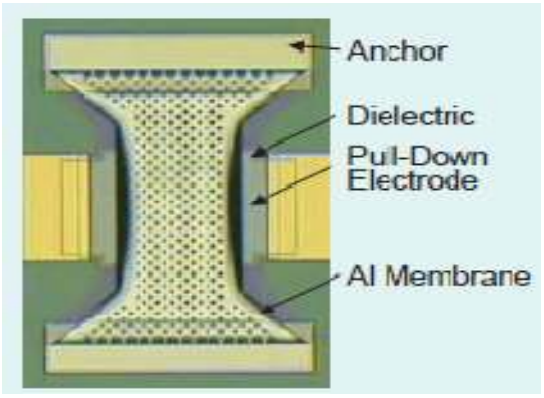


Fig. 2.4: Raytheon capacitive shunt switch [44].

Fernandez –Bolanos et al. proposed RF MEMS capacitive switch with low actuation voltage with excellent capacitive ratio close to 200 using TiO_2 as dielectric as shown in Fig. 2.5. This design uses low loss high resistivity silicon substrate [45]. It has an insertion loss less than 0.5dB and isolation more than 20dB at 20GHz at a low actuating voltage of 8V. *This reported work on switch lacks the study on parameters such as spring constant and*

restoring force. Keeping in view the low actuation voltage these parameters become critical for long term operation.

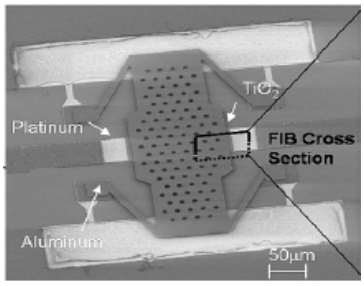


Fig. 2.5: SEM View of the MEMS switch [45].

S. Pacheco et al. of the University of Michigan presented a low spring-constant membrane capacitive switch [46]. The membrane is connected using a folded spring to the anchors and the spring constant can be lowered to 1-3N/m with the use of several turns as shown in Fig. 2.6. This result in a pull-down voltage of 8-15 V and a relatively low switching speed of 30-40µs. Since the restoring forces are low for such a design, these switches are useful when integrated with a pull-up electrode placed 1-2µm above the movable membrane. Another X and K band SPDT switch was also developed using the same configuration [47]. *It has been mentioned in the study that the problems with low spring constant is their sensitivity to mechanical forces such as acceleration, vibration and the associated slow response times.*

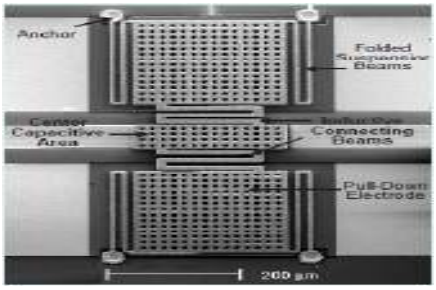


Fig. 2.6: Low spring-constant MEMS switch [46].

The LG KOREA developed a very-high-capacitance-ratio MEMS shunt switch [48-49] as shown in the Fig. 2.7. The design is based on the standard fixed–fixed beam capacitive shunt switch and uses strontium-titanate-oxide (SrTiO3) as the dielectric layer. STO results in

a relative dielectric constant of 30–120 with a low loss tangent (0.02) and very low leakage current. The fabricated switches achieved a capacitance ratio of 600 and a down-state capacitance of 50 pF (up-state capacitance of 70–80 fF). The pull-down voltage of 8 V has been reported due to the low-spring constant support structure. The switch isolation is better than -40dB at 3-5 GHz. *The reported work does not explain the effects of low pull-in voltage for the stable operation of the switch.*

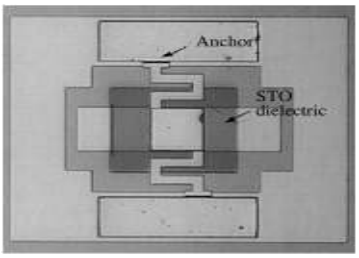


Fig. 2.7: LG-Korea high-capacitive-ratio MEMS shunt switch [49].

S C Shen et al. of University of Illinois developed a low-voltage DC-contact shunt switch [50-51].The low-voltage design is achieved using narrow low-spring constant support beams near the membrane anchor. The switch consists of two pull-down electrodes on both sides of the center portion of the switch as shown in the Figure 2.8. The actuation electrode area is (2) x 800 x 100 mm^2 and the resulting pull down-voltage is 9–16 V.

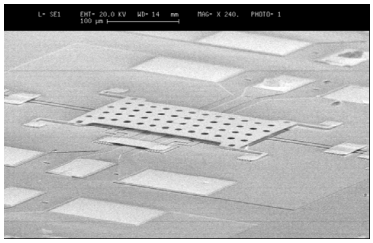


Fig.2.8: SEM view of DC-contact MEMS shunt switch of University of Illinois [51].

Richard Chan et al. of University of Illinois investigate the performance and lifetime of a metal-to-metal shunt RF MEMS switch fabricated on an SI–GaAs substrate [52-53]. The reported switch is a shunt bridge design that is compatible with standard microelectronic processing techniques. The RF performance of the switch includes isolation better than 20 dB

from 0.25 to 40 GHz and switching speeds of less than 22μs with actuation voltages less than 15V. The switch structure includes separation posts that eliminate sticking failure and has demonstrated lifetimes as high as $7x10^9$ cold switching cycles. These results show that good reliability is possible with a metal-to-metal RF MEMS switch operated with a low actuation voltage.

V Milanovic et al. of University of California, Berkeley developed a process for the transfer of MEMS switches from a low-resistivity silicon substrate to a quartz substrate [54-55] as shown in the Fig. 2.9. This allows the MEMS switches to be fabricated using standard CMOS techniques and then transferred to a microwave-compatible substrate. They have developed three switches using this technique: a DC-contact series switch using a fixed–fixed beam design and a DC-contact shunt switch. The actuation voltage varies from 30 V to 110 V and it is due to chip-to-chip variation in the height of the transferred MEMS structures.

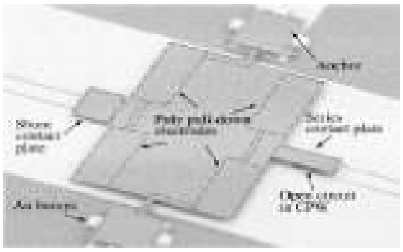


Fig. 2.9: Berkeley see-saw series/shunt MEMS switch [54].

S Pranonsatit et al. of Imperial College London, U.K [56] demonstrated single-pole eight-throw radio-frequency (RF) MEMS rotary switch, the concept of this rotary switch is based on the adaptation of the axial gap wobble motor [57]. A prototype switch has been made using separately fabricated stator, rotor, and cap components that are then assembled. An average contact resistance of 2.5 was recorded. However, values as low as 1.0 was also found. The assembled rotary switch demonstrated an excellent RF performance. With the inclusion of feed lines, the insertion loss was 2.65dB at 20 GHz after renormalizing the measurement

reference impedance. When the loss of the feed lines is subtracted, the worst-case ON-state intrinsic insertion loss of the rotary switch is only 2.16 dB at 20 GHz.

Chia-Hua et al. of National Taiwan University achieved low pull-in voltage and high isolation of the switch by exploiting buckling and bending effects induced by well-controlled residual stress [58]. The minimum actuation voltage of the fabricated switch was measured to be 10.2 V. They achieved insertion loss and isolation of 0.21 dB and - 44 dB respectively at 5 GHz. Figure 2.10 shows the SEM image of their switch.

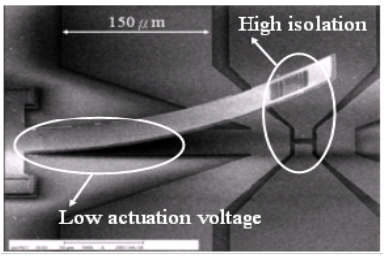


Fig. 2.10: Switch from National Taiwan University using controlled residual stress.

M. Tang of Nanyang Technological University, Singapore fabricated a shunt switch by forming a basin in silicon which partially defines the gap between membrane and down electrode for X-band application [59]. In this configuration, the ground line was restricted from the basin. Figure 2.11 (a) and (b) shows SEM views of their switch where single and double bridge was fabricated to achieve the high isolation at resonant frequency. They achieved the isolation loss of 16.5-28dB and 25-35 dB for the single and double bridge respectively in the frequency range 10-13GHz and a pull-in voltage of 20.4V.

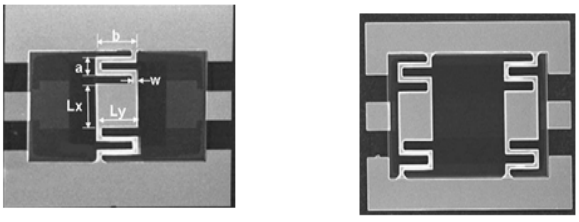


Fig. 2.11 : Nanyang Technological University shunt switch in (a) single bridge (b) double bridge configuration.

Wei-Bin Zheng of Southeast University Nanjing, China fabricated shunt RF MEMS switch for X-band application on GaAs substrate [60]. They achieved an isolation of -42dB at self resonant frequency of 24.5 GHz. The insertion loss between 1 to 25.6 GHz was less than 0.25dB and actuation voltage was 17V. They demonstrated life time as long as $5x10^5$ cycles.

Puyal et al. of Centre National de la Recherche Scientifique (LAAS-CNRS) France, [61] presented the scalable shunt switches models with different sizes ranging from 350x340 μm^2 to 800x1000 μm^2 for varying resonant frequencies. The insertion loss in the range 1.1 dB to 0.3dB was reported up to W band with actuation voltage ranging from 20 to 35V. The SEM photos are shown in the Figure 2.12 with holes on the beam. *The study does not explain the effect spring constant effect arising due to the change in mass because of dimensions and holes variation in the beam.*

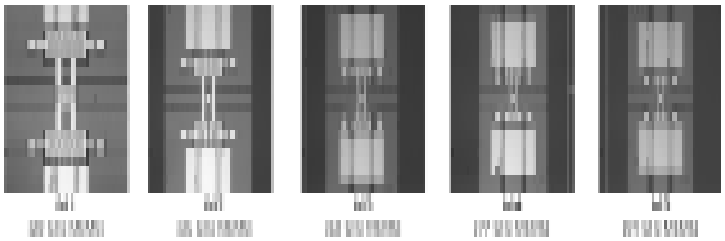


Fig. 2.12: SEM images of differnt configurations [61].

H. U. Rahman et al. of University of New South Wales, Australia [62] presented a simple low actuation voltage series switch at 6.39V as shown in the Figure 2.13. The low actuation voltage has been achieved by varying the cantilever dimensions. *This work does not cover the effect of very low actuation voltage on the restoration force which has a direct bearing on the stable operation.*

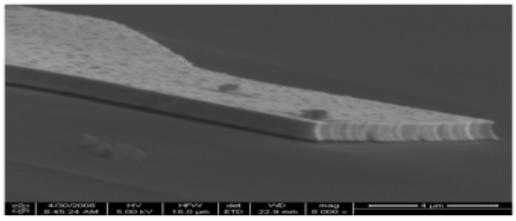


Fig. 2.13 : SEM image shows the cantilever of the switch.

They also fabricated the non standard cantilever beam designs [63]. A mechanical modelling was presented based on the Euler–Bernoulli beam equations. The SEM photo is shown in the Figure 2.14. The fabricated switches using these cantilever beams exhibited 23V actuation voltages using a dry-release technique. The isolation was better than 27dB, from 0 to 40GHz. The insertion loss of 1.3dB was achieved and results were not in consonance to simulated performance in terms of insertion loss. *This is high insertion loss which does not exploit the MEMS technology advantage. The emphasis on the spring constant was concentrated and does not include the stress analysis on the cantilever.*

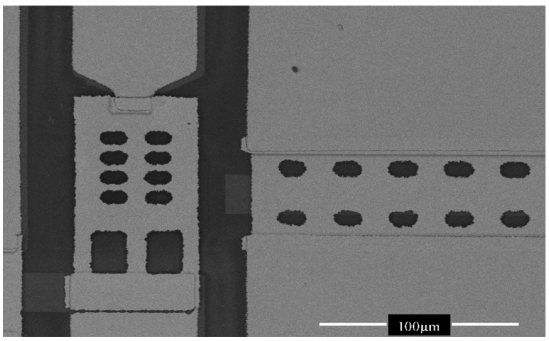


Fig. 2.14: SEM image shows the top view of the switch [63].

Based on above exhaustive literature survey we found that there is need to address some of technology issues more thoroughly, such as high restoration force for low pull in voltage, stress effect, easy removal of sacrificial layers and in-built reliability of MEMS switch through design. Brief details and associated challenges are discussed in following section-

Pull-in voltage in the electrostatic actuation of the RF MEMS devices is a significant parameter. A low pull-in potential has many advantages. Mainly it allows the switches to be easily integrated with additional circuitry as it reduces the burden of resorting to voltage boosting circuits and saves precious substrate area. Secondly, it reduces the power dissipation which is proportional to the square of the voltage between the signal line and membrane in the down-state. Most significantly, a low pull-in voltage improves the reliability as there is

less charge injection into the insulting layer due to reduction in electric field across it [64] in the down-state of the switch. This charge in the insulating layer alters the pull-in voltage and in the extreme case may result in the switch being permanently in either the upper or lower state by keeping switch permanently on or off. This is a serious reliability problem of capacitive switches. C. L. Goldsmith et al. reported that the lifetime of capacitive switches strongly depends on the actuation voltage [65]. Reduction in pull-in voltage also allows lesser insulator thickness resulting in higher capacitance in the "OFF" state (C_{off}). This improves the C_{off}/C_{on} ratio of the switch, thus improving the device performance. *Thus in this work, low pull-in voltage structures with sufficient restoration force for capacitive shunt-type and ohmic series switches have been considered for study.*

It is known that a low pull-in voltage [66] can be achieved by reducing the gap between the signal line and membrane, or by increasing the effective overlapping area between membrane and bottom electrode or by designing a membrane of low spring constant [67]. While reducing gap or increasing overlap will increase insertion loss due to increase in C_{on}, reducing the spring constant (K) of the membrane presents more flexibility [68] in achieving low pull-in voltage without affecting the switch performance at higher frequencies. The design of membranes of low spring constant to reduce pull-in voltage at the cost of restoration force is a serious concern. Moreover, release of a membrane of low spring constant is difficult due to stiction forces. *We undertake this challenge in our work by novel design of switch structure.*

Any Stress in the released membrane is major issue for all MEMS application. The type and the quantity of the stress changes from design to design, process to process and the also depend on material of the membrane. The beam or cantilever design is the key factor for stresses which can result after the fabrication. The mechanical design and analysis are to be uniquely carried to have built-in reliability. A compressive stress in a membrane may permanently close the switch whereas a tensile stress may increase the pull-in voltage of a

membrane. As we have already discussed that a high pull-in voltage of membrane can lead to a charge injection in dielectric material and hence affect the reliability of the switch in long run. So the material properties of the membrane should be characterized thoroughly in same ambient condition before it has to be used in actual device fabrication. So overcome this challenge selection of the test structures and characterization techniques should also be done appropriately to achieve accurate results. *In this work, the actual design of the membrane is used to minimize the effect of stress on the membrane*.

2.2 RF MEMS Phase Shifter

A phase shifter [69] is a two-port network with the provision that the phase difference between output and input signals can be controlled by a control signal, usually dc bias. Phase shifters with low insertion loss, low drive power, continuous programmability and low production cost are the key to the development of lightweight Active phased array systems. Currently Phase shifters are based on ferrite materials, pin diode and FET switches. Each type has its own advantage in terms of power handling and switching speed etc. The p-i-n based devices consume more dc power while solid state type incurs high insertion loss. Solid-state phase shifters provide a good planar solution at microwave frequencies and have been extensively used in modern phased-array systems. Whereas MEMS type phase shifters are finding its place due to its technical superiority in terms of very low insertion loss, virtual no power consumption, high linearity and bandwidth. In general the micro-electromechanical phase shifters under development are based on the MEMS based switches which have replaced the solid state switches. MEMS switches incur low loss and these have very low up state capacitance which results in a wide band performance when compared to similar designs using solid state devices.

2.2.1 RF MEMS Phase Shifter Configurations

Most of RF MEMS phase shifters developed are based on the established designs except that the solid-state switch is replaced by a MEMS switch. The preferred approaches are discussed in this section.

In case of the **distributed type** t-line is periodically loaded with the variable capacitors. The change in capacitance influences the phase velocity of traveling electromagnetic wave causing a phase delay and thus acts as delay line. The distributed approach consists of a high impedance line (> 50 ohm) which can be easily implemented using coplanar waveguide as shown in Fig. 2.15 [70-71]. The periodic spacing and the number of bridges depend upon the design. The key technology developments for realization of DMTL delay line are actuation mechanism and the precise control of processes, as transmission line properties are sensitive to geometric tolerances. For given substrate and frequency band phase shift can be varied by difference of loaded line impedance [72]. In general DMTL approach is preferred for 30GHz and above.

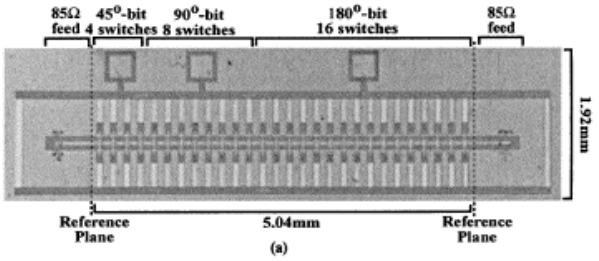


Fig. 2.15 : Distributed transmission line digital phase shifter [72].

The **reflect line** phase shifter can be implemented using a succession of MEMS series or shunt switches on a transmission line. The reflect-line design results in double the phase delay per unit length as compared to the standard design [73]. The electrical separation between the switches is thus equal to the half of the lowest resolution bit. Figure 2.16 shows the general approach of the reflect line phase shifter configuration. The coupler needs larger area for realization along with MEMS switches.

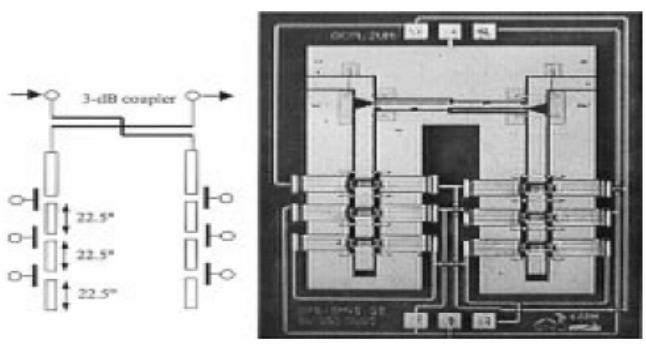


Fig. 2.16: Configuration of the reflect line phase shifter [73].

Loaded line phase shifters are designed by loading t-line with two different impedances and use a midsection matching network [74-75]. Figure 2.17 shows the sketch of the loaded line design topology. The matching network ensures that phase shifter is matched to Z_o for both loading conditions. Loaded line phase shifters yield excellent performance for small phase delays like 11.25° and 22.5°. The higher bit design does not provide accurate results in terms of phase control. The loaded line phase shifters can be cascaded in series to result in any required phase shift due to their perfect match. RF MEMS switches can be used to load the line.

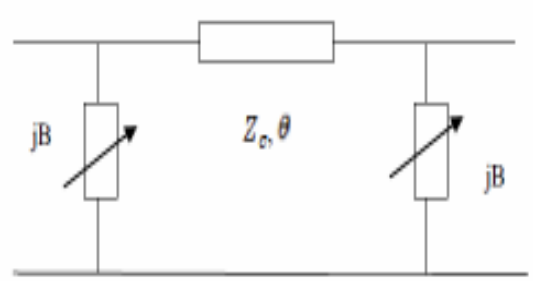


Fig. 2.17: Loaded line phase shifter configuration [74].

Switched line is one of the most adopted topology as it can achieve the digital phase shifter by using switched delay line technique. In this approach each delay bit is implemented separately and an N bit phase shifter is designed using a succession of several bits of different values [76-77]. The phase delay is obtained by switching in the required number of bits. Switched line phase shifters can be fabricated using series or shunt switches. A sketch of the

four bit is shown as below in the Figure 2.18. A 'T' junction at the input and the output is connected through the transmission line via MEMS switches.

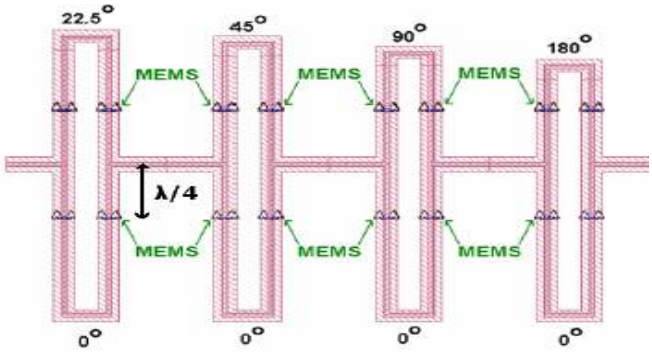


Fig. 2.18: Switched line phase shifter configuration [76].

The lower part is shown as the reference path with two switches in each bit. The upper path or the delay path is connected through the switches in the similar way. The signal passes through the reference path when these switches are in 'ON' state and upper path switches are in the 'OFF' state and vice versa.

2.2.2 RF MEMS Phase Shifters- Technology development

RF MEMS Phase Shifters find application in airborne and space-borne radar sensors which do not require long range search and track capability. The low-altitude unmanned aerial vehicles offer potential for RF MEMS Phase Shifters. Unlike RF MEMS resonators, RF MEMS Phase Shifters have not been commercialized. The initial MEMS Phase Shifters research companies include Raytheon, DARPA, MEMTronics, Radant MEMS, Wispry and XCOM wireless. The most required applications are in the frequency bands namely X, Ku, Ka, V and W for the RF MEMS Phase Shifter development. The switching time of MEMS type phase shifters is of the order of 1-50 μs which allows them to be used virtually used in all systems except fast switching speed required systems. The following is the literature details of earlier work done on the RF MEMS Phase Shifters.

Raytheon developed 2 bit and 4 bit X band MEMS Phase shifters using reflect line topology on 500µm Si/Al_2O_3 thick substrate [78]. The reported average insertion loss was 0.65 dB and 1.15 dB respectively with phase error of the order ± 11 degree. The die area for the 2 bit is 50 mm^2 and 100 mm^2 for 4 bit.

B. Pillans et al. reported ka band phase shifter (32-36 GHz) using switched line topology [79]. He reported average insertion loss of 2.25 dB with phase error 13 degrees. The image is shown in the Figure 2.19. *Above works have high phase error and the large substrate area*.

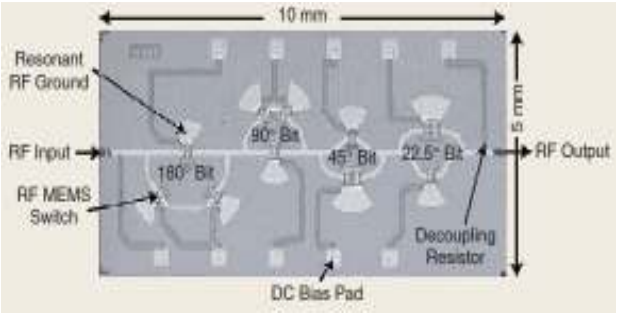


Fig. 2.19: Raytheon phase shifter [79].

Rockwell reported a pioneer work using series (SP4T) switched line topology on 200µm GaAs substrate [80-81]. The average insertion loss was 0.6 dB and 1.1 dB for the 2 bit and 4 bit types.

J.F DeNatale developed 35-50 GHz 3 bit phase shifter with 2.2 dB insertion loss fabricated on 75µm GaAs substrate using switched line topology [82]. *The 75µm substrate lack integration to other devices and lead to higher insertion loss.*

Rockwell Science Center developed a 4-bit DC-40-GHz True Time delay network phase shifter using metal to metal contact RF MEMS switches [83-84]. The phase shifter is built on a 75-µm-thick GaAs substrate. The average insertion loss is -2.2dB at X-band. The study suggested that loss improvement to -1.4 dB for the 4-bit design if the phase shifter is

integrated on a 200-μm GaAs substrate. The area of the 4-bit X-band phase shifter is 30 mm^2. Figure 2.20 displays the image of the die.

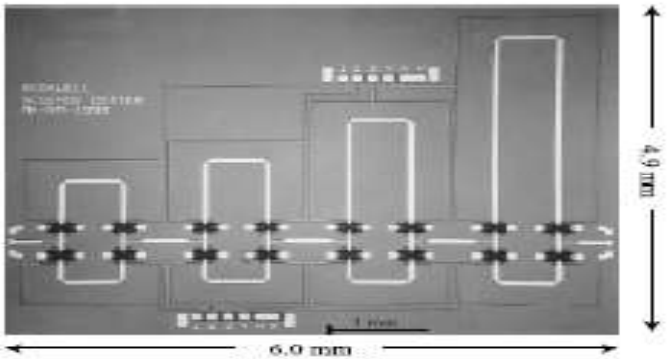


Fig.2.20: Rockwell DC-40 GHz switched line phase shifter [83].

Nanjing Electronic Devices Institute China presented a development work in X-band by fabrication of the compact 5-bit Switched Line Digital MEMS Phase Shifter on HRS with overall chip size of 7mm x 4 mm [85]. He reported using 3 port MEMS switch resulting into a compact design. The Phase shift error is within 5° and insertion loss is 3.6 dB at 10 GHz. *There is a scope of improvement in terms of the insertion loss with phase error with in 3° in this frequency range. The photo is shown in the Figure 2.21.*

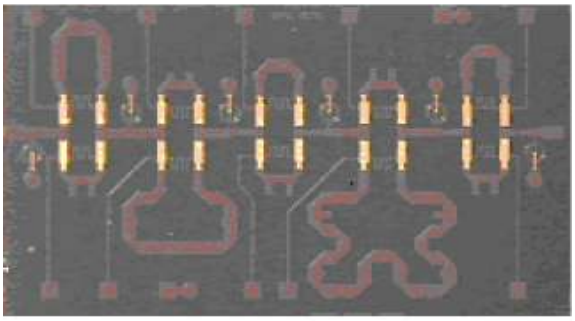


Fig. 2.21: Nanjing Institute phase shifter [85].

University of Perugia Italy presented a pioneer work of design and manufacturing of a 5 bit K-band MEMS phase shifter by employing different switch configurations namely cantilevers and air bridges in the form of SP2T and SP4T at RF junctions [86-87]. These were fabricated monolithically using 200μm thick HRS at FBK foundry. The three

configurations were optimized and SP2T based option found to be best trade off. It is reported that this option has the insertion loss of 2.2 dB with insertion loss variation within ±0.4 dB with foot print area as 6.5x3.2mm^2. They also presented the packaging of the phase shifter die and reported an addition of insertion loss of 1.8dB at 20.7 GHz. *The packaging loss is higher in comparison to the phase shifter insertion loss and there is scope of packaging optimization for electrical performance.* The image of the die is shown in the Fig. 2.22.

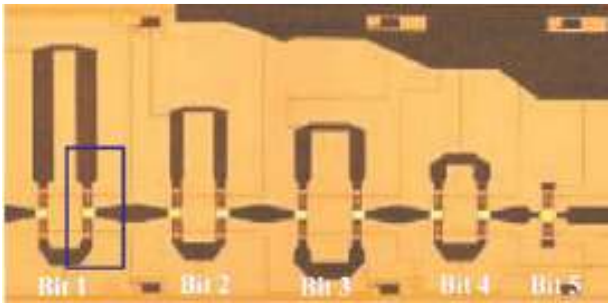


Fig. 2.22: Image of the University of Perugia phase shifter [87].

GAO Yang et al. fabricated a 4-bit MEMS switched-line phase shifter which is composed by MEMS SP4T switches and micro-strip transmission lines and works in X-band [88]. Each MEMS SP4T switch is used to switch two different signal pathways, reference phase signal pathway and delayed phase signal pathway. Each MEMS SP4T switch consists of 4 contact type RF MEMS switches with cantilever beam movable contact structure. The simulation results show that the return loss and insertion loss of SP4T switch are -36 dB and -0.18 dB at 10 GHz respectively. Figure 2.23 shows the image of the phase shifter.

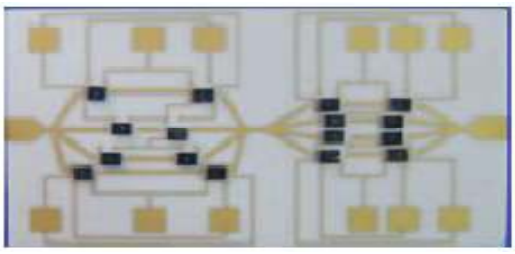


Fig. 2.23: Hybrid integrated 4-bit MEMS switched-line phase shifter [88].

Young J Ko et al. designed an integrated 3-bit RF MEMS phase shifters comprising of the three different 1-bit phase shifters with 11.25°/22.5°/45° stub-loaded line phase shifters [89]. The fabricated 3-bit phase shifter has insertion loss of avg. -2.0 dB and return loss of min. -10dB with phase error of average 2.0° at the frequency ranged between 10.7-12.75 GHz. The die size of 25 mm^2 has been reported.

Robert Malmquist et al. designed a 4 bit digital type MEMS phase shifter and optimized for 35 GHz [90]. This design has been implemented on a 525 µm thick quartz substrate. The two smallest bits are implemented using loaded-line techniques whereas the two largest bits are made using switched delay lines. The circuit area is 5x l1 mm^2.

Nickolas Kingsley et al. presented a 4-bit MEMS phase shifter fabricated, integrated, and packaged into an organic flexible low-permittivity material [91]. A microstrip switched-line phase shifter has been optimized at 14 GHz for small size and excellent performance. In addition, the MEMS phase shifter was packaged in an all-organic flexible low permittivity liquid-crystal polymer (LCP) package. For the 4-bit phase shifter the worst case return loss is greater than 19.7 dB and the average insertion loss is less than 0.96 dB. The reported average phase error is 3.96°.

Songbin Gong et al. developed a 2-bit switched-line phase shifter using dc-contact single-pole four-throw (SP4T) RF micro-electromechanical switches at 60-GHz [92]. The phase shifter demonstrates an average insertion loss of 2.5 dB in the 55–65 GHz band with a return loss better than 12 dB for each state. The phase error for each state of the switched-line phase shifter is less than 1° at 60 GHz. Figure 2.24. Shows the image of the 2 bit phase shifter developed.

JS Hayden et al. of University of Michigan fabricated a 2-bit Ka-band distributed phase shifter on a quartz substrate using coplanar waveguide (CPW) lines and RF MEMS capacitive switches [93-94]. The developed phase shifter is shown in the Fig. 2.25. The

phase shifter consisted of 21 sections with a spacing of 400 μm resulting in a total length of 8.4mm.

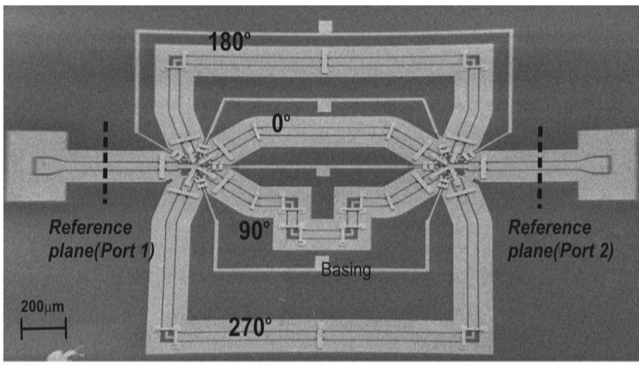


Fig. 2.24: SEM images of the fabricated V -band 2-bit phase shifter [92].

The performance of distributed phase shifters is strongly dependent on Q of the loading capacitor. This was achieved using metal-air-metal capacitors at Ka-band frequencies. The 2-b phase shifter results in an average insertion loss of -1.5 dB.

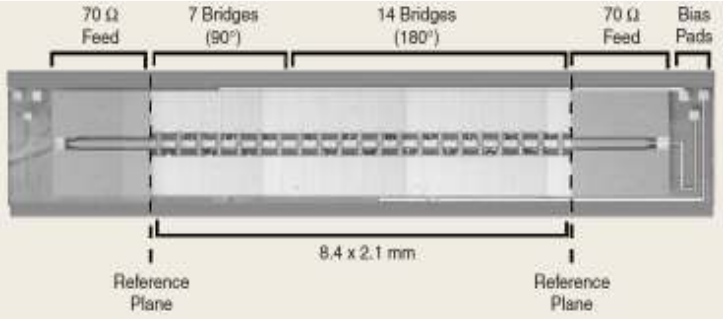
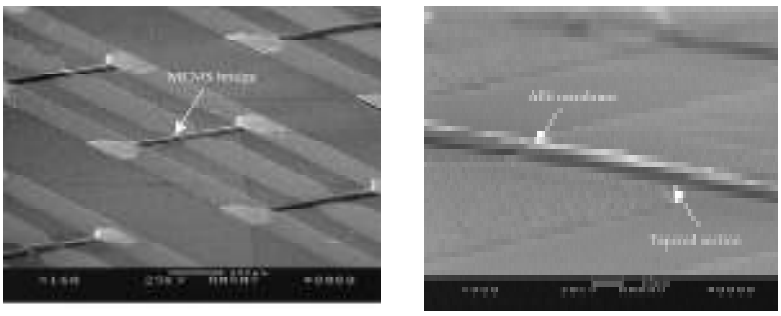


Fig. 2.25: University of Michigan DMTL phase shifter [94].

Jian Qing et al. describes the design, fabrication, and testing of distributed MEMS phase shifters for Ka-band communication systems [95]. The phase shifters are fabricated on the high-resistivity silicon substrate using suspended AlSi bridge membrane. The up state insertion loss is 0.84 dB at 30 GHz and 1.75 dB at 40 GHz. The return loss is greater than 10 dB from 0-40 GHz range The measured results demonstrate a phase shift of 286° at 36 GHz with the actuation voltage of 25 V and a return loss better than 10 dB over 0–40 GHz band. Figure 2.26 shows the SEM Image of the (a) entire structure (b) and the cross section.



(a) (b)

Fig. 2.26: SEM Image of the (a) fabricated phase shifter structure and (b) cross section of the Membrane [95].

Based on the RF MEMS exhaustive literature survey a summary of RF MEMS phase shifters developed by various researchers in different frequency bands with details such as types of configurations, insertion loss, and number of bits, design topology, phase accuracy and the chip area is presented in Table 2.1.

It is evident from above literature survey that there is lack of systematic study in 5-bit phase shifter in Ku band which is very strategic requirement for defense application. Therefore, there is a need to develop high resolution (≥5 bits) Ku- band MEMS based phase shifter, which we undertake in this work.

Table 2.1: Comparison of RF MEMS Phase Shifters Performance of Different Groups

Frequency (GHz)	No. of bits	Insertion loss	Design Type / Substrate	Phase Accuracy	Chip Area	Reference
7-11	2	0.65dB	Reflect Line 500 µm	± 11 deg.	50 mm^2	[78]
7-11	4	1.15dB	Reflect Line 500 µm	± 11 deg.	100 mm^2	[78]
32-36	4	2.25dB	Switched Line 150 µm Si	13 deg.	50 mm^2	[79]
10-18	2	0.85 dB	Switched Line 200 µm GaAs	±2deg.	12 mm^2	[80]
8-12	4	1.6 dB	Switched Line 200 µm GaAs	± 4 deg.	21.3 mm^2	[81]
35-50	3	2.2dB @ 35 GHz	Switched Line 75 µm GaAs	± 6 deg.	16 mm^2	[82]
10-40	4	2.6dB	TTD	± 4 deg.	8.4 mm(L)	[83-84]
9-11	5	3.6dB	Switched line 200 µm HRS	< 5 deg.	28mm^2	[85]
20.2 – 21.2	5	3.5dB	Switched line 200 µm HRS	< 2 deg.	20.8mm^2	[86-87]
10.7- 12.7	3	2 dB	loaded line	±2deg.	25 mm^2	[89]
35	4	2 dB	loaded line / switched line	---	55 mm^2	[90]
14	4	0.96	switched line	3.96°	66.78 mm^2	[91]

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CHAPTER 3

RF MEMS Switch Design Configurations & Simulation Results

There are various design configurations reported in the literature for the capacitive shunt and ohmic series type of switches. The goal of this chapter is to evolve a design configuration which has the built in reliability by optimizing the various features to ensure stable operation of the switches [96-98]. The complete details of design and simulation results are presented in the following sections.

3.1 Design Topology for built-in reliability of different Configurations

A split beam concept has been evolved uniquely in comparison to the holes commonly available in the literature. This has been implemented to overcome the various criticalities of restoration force for stable operation and the advantage of the structure release due to large split area during the release process. In fact, it has been emphasised to achieve the higher spring constant with lower structural stress arising due to the structure design. A complete analysis of the spring constant and the stress was carried out to address the long term operation.

3.1.1 Design Flow

The design flow as shown in the Fig. 3.1 has been evolved for the development of the both type of RF MEMS switches under this work. It begins with the goals for the electrical

and mechanical specifications. Process inputs from the foundry in terms of process capabilities like metallization method and thickness, sacrificial layer characteristics, bridge deposition procedure and release process are taken into account during the design and modelling. After the model generation, the full wave electromagnetic and electro-mechanical analysis has been performed leading to the circuit level simulation. The decision for mask generation shows the confirmation of meeting the requirement specifications. The fabrication of structures and the devices is followed by the mask generation. A simplified cross sectional view and electrical schematic of capacitive shunt and ohmic series switch are shown in Figs. 3.2 (a, b) and 3.3 (a, b) respectively.

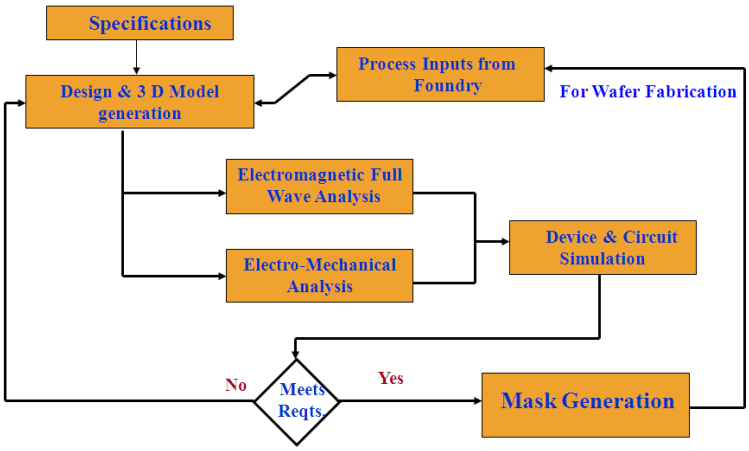
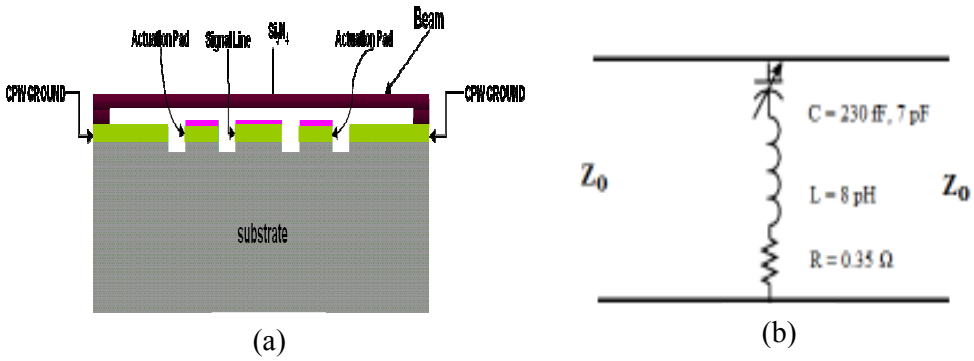


Fig. 3.1: Flow for Design, Simulation and Device Development



(a) (b)

Fig. 3.2: (a) Cross section for shunt capacitive switch and (b) electrical equivalent.

In case of shunt configuration, the electro statically actuated switch consists of a conductive fixed-fixed beam supported by the anchors between the two sections of ground in a coplanar waveguide (CPW) [99]. In this case, parasitic capacitance limits the performance when the switch is in the up state by the unwanted reflections. In order to isolate the dc control voltage from the RF, this design uses separate electrodes for the actuation of the membrane. The bridge can be brought close to the conducting line by the application of sufficient bias voltage through the actuation electrodes. For simple structures this is determined by making use of the force balance equations between the electrostatic pull down and mechanical restoring forces on the bridge.

The series switch [100] is developed as shown in Fig. 3(a) for the cross sectional view with cantilever having the anchor pad on the one side of the transmission line and discontinuity in the RF line. The actuation pad is covered with the silicon nitride dielectric to avoid the direct contact of the RF and actuation potential. This avoids the hard contact of the actuated cantilever with the dc electrode. The MEMS cantilever is modelled by a series capacitor-inductor-resistor combination as shown in the Fig. 3.3 (b). The values shown for the capacitor, inductor and the resistance have been extracted for the model used for the development.

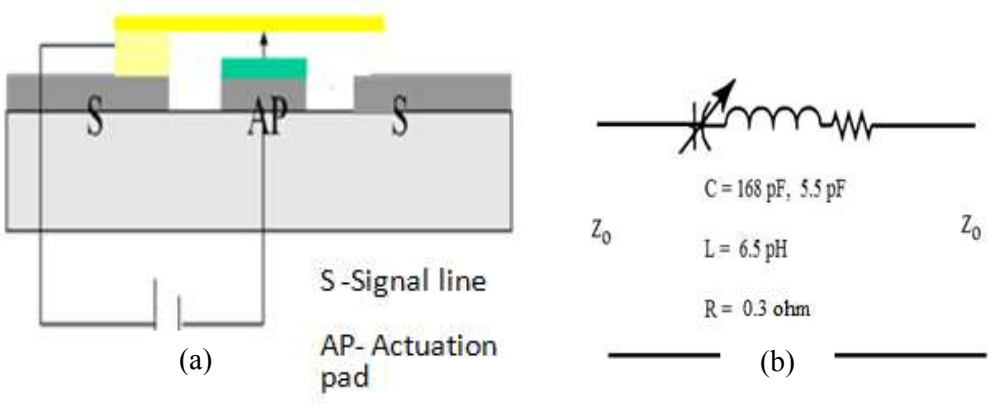


Fig. 3.3: (a) Cross section for ohmic series switch and (b) electrical equivalent.

3.2 Design topology and Simulation

3.2.1 Split Beam Capacitive Shunt Configuration

The primary emphasis of this work was to design the capacitive shunt MEMS switch configuration with split membranes for low force with electrostatic actuation and sufficient restoration force. Two configurations i.e. having DC bias pads on both sides and only one side were designed. Both these configurations have been provided the symmetric actuation along the RF line for uniform pull in. The configuration having single bias pad was conceived for simple implementation of the switch in the systems during practical application. Single bias pad has lot of ease in applying the DC potential in comparison to the two bias pad configurations however this needed to create a discontinuity in the RF line. The discontinuity has been provided in the single DC bias pad design in view to study its effects on RF performance. The RF line is connected through the air bridges over the DC line. All other design parameters have been exactly same in both the configurations. Both the configurations have bias pad on the periphery so that smaller length of bond wire is sufficient during assembly and packaging to avoid the parasitic effects at high frequencies. Fig. 3.4 (a) and (b) shows the top view of both the configurations. The CPW of 50Ω impedance with Ground/Signal/Ground (GSG) configuration was used for design.

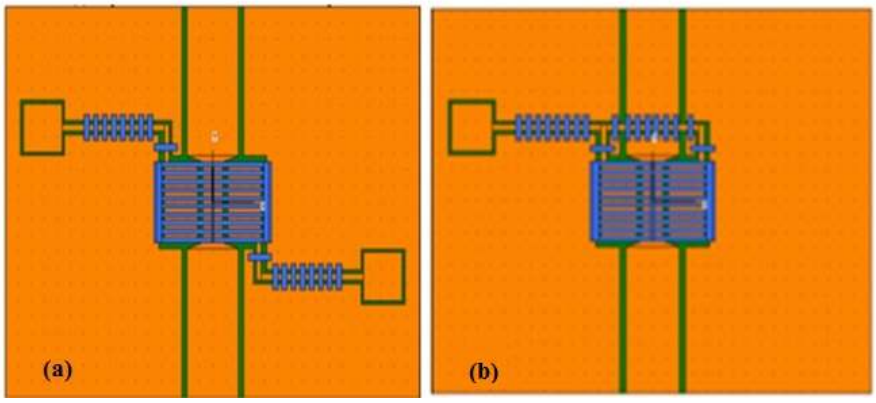


Fig. 3.4: (a) Top view of the two side dc bias pad and (b) single dc bias pad.

Figure 3.5 shows the cross section of the shunt switch displaying all the dimensions of the beam and actuation area. The actuation pads have 130 x 250 μm^2 area. The thickness of the CPW and actuation electrodes is 3.0 µm. The actuation electrode and RF line has been deposited with 0.1 µm silicon nitride. The anchors have foot print area 20x20 μm^2 area. The beam length is 436 µm including anchors.

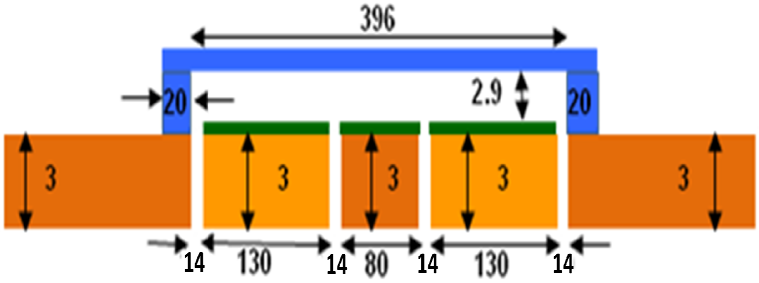
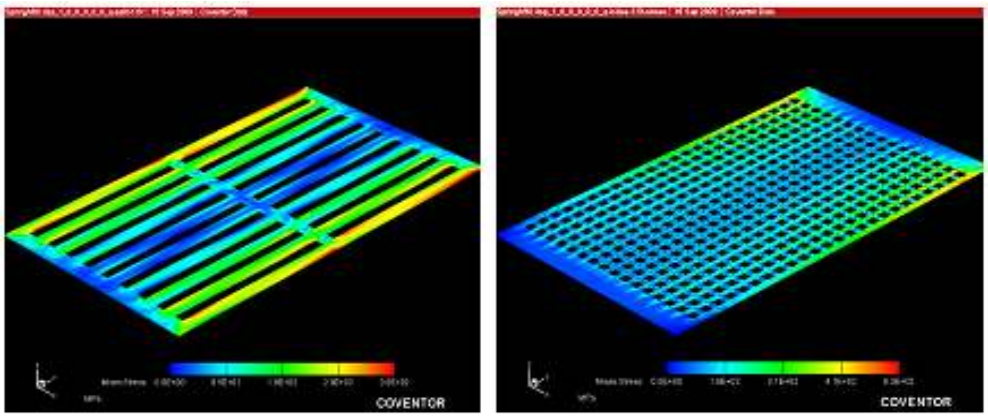


Fig. 3.5: Cross section of beam area with actuation pad. All dimensions are in µm.

The split beams in rectangular shape instead of holes from other reported work has the advantage of low stress across the beam making it more robust to the environmental effects like vibration and shock. The other advantage is the ease in structure release due to continuous larger area available for etchant percolation. Figure 3.6 (a) and (b) shows the 3D models of the split beam and rectangular holes analyzed with FEM for stress analysis. The Beam outer dimensions have been taken as same for both the configurations except for the internal structural design. The mass of the beam structure also has been maintained same for both the configurations so as to analyze the proposed split beam structure with respect to the rectangular holes structure. The holes dimension is 10x10 μm^2 and the edge to edge gap between the holes has been optimized in order to achieve the same mass as of the split beam structure.

The membrane details with respect to dimension and gap are given in the Table 3.1. The analysis shows that the stress of the order 630 MPa in case of rectangular holes and 380 MPa for the split beam configuration has been observed. The stress analysis shows the

superiority of split beam design with respect to the rectangular holes. CoventorWare has been used for the simulation and analysis.



(a) (b)

Fig.3.6: (a) and (b) Stress analysis 3D models for the split and rectangular holes beam respectively.

Table 3.1: Dimensional details for the membrane

Beam Details	**Parameters**	
Dimensions(μm)	Length :396 Width: 249	Thickness 1.5
Type	Split	Rectangular holes
Stress (MPa)	380	630
Stress Area between split beams/holes	178 x11 μm^2	10x10 μm^2
Array size	9x2	22x16

For the proposed structure, the 3D full wave electromagnetic simulation was carried out by a finite element method using Ansoft HFSS. Figure 3.7 shows the effective length of the membrane and the points at which pull in force is applied due to underneath placement of actuation electrodes on both sides for symmetric actuation. The effective beam has length of

396µm.The EM simulation results of RF parameters such as isolation, return and insertion loss are shown in comparison to the measured results in the the experimental section.

Fig. 3.7: Dimensions for the reduced model excluding anchors.

3.2.2 Electromechanical Simulation Results

A 3D model in CoventorWare is generated using customized process. Device fabrication method was implemented for the structure feasibility. A 2D layout was generated for each and every mask pertaining to the fabrication steps of the device. Finally both, the fabrication flow and 2D mask layouts were integrated to generate the 3D model of the device. The analysis has been done through finite element method using manhattan meshing and the beam was fixed at the extreme ends. Further the membrane was allowed to deform with respect to the application of gradual increase in voltage. The electromechanical simulation result for the pull in voltage is shown in the Fig. 3.8.

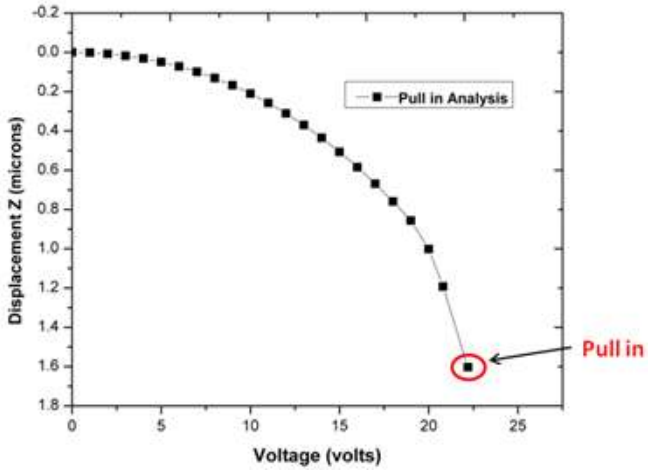


Fig. 3.8: Voltage versus displacement curve for pull-in.

A nearly linear deflection has been obtained for a travel of 1.6µm at a voltage of 22.2V up to the pull in point. Beyond the pull in voltage point a sudden snap down was observed. The membrane was analyzed for the hysteresis response which is quite crucial for the stable operation of the switch. Figure 3.9 shows the contact point at the 24.3V having air gap as 2.9µm. The pull back phenomenon also called restoration force, occurred at the 17V after removal of the actuation potential. The pull back shows that the design has the sufficient restoration force required for the stable operation of the device.

The membrane was split into ten strips each having width of 15µm and gap of 11µm. This was optimized keeping in view the air damping and the easy removal of the sacrificial layer during the fabrication of MEMS switches.

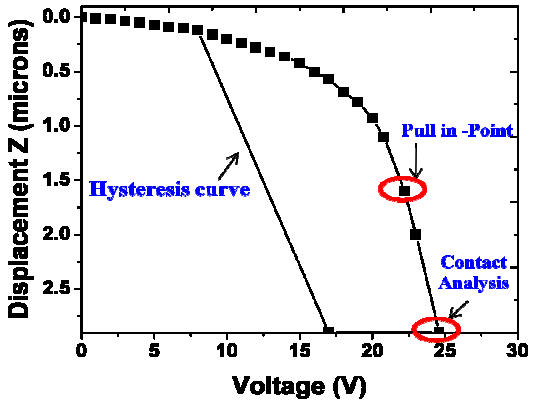


Fig. 3.9: Contact and Hysteresis analysis curve.

The pull in voltage was calculated using the equation (1)

$$V_p = \sqrt{\frac{8kd^3}{27\varepsilon A}} \qquad (1)$$

Where k = Spring Constant

d = gap between electrodes = 2.9 µm

A = Area of electrode

ε = permittivity of air

Spring constant has been calculated using equation (2) for the membrane

$$k = 16EW\left(\frac{t}{l}\right)^3 \quad (2)$$

Where t = Thickness of membrane = 1.5 µm

E= Young's Modulus = 79 GPa

W = width of the beam

Based on the model values used in equation (2) the spring constant was found to 17.17 N/m for the fixed-fixed beam. This value was inserted in equation (1) and the pull in voltage was calculated as 20.76V. By simulation the pull in voltage was found to be 22.2V. A 3D view of the Membrane deflection is shown in the Fig. 3.10. The maximum deflection has been observed at the centre of the membrane which is required for the proper contact at the centre of the transmission line.

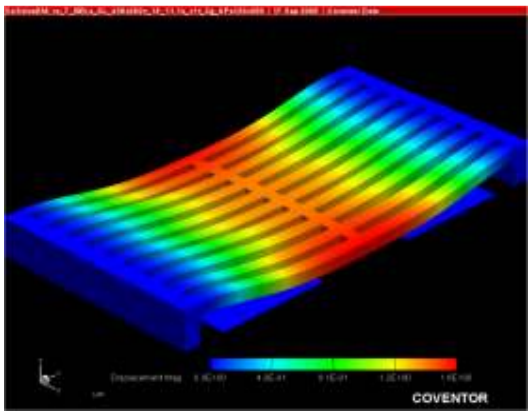


Fig. 3.10: A 3D model of beam under pull-in and contact analysis.

The mechanical resonance is significant from the structural integrity point of view. Membrane was split into smaller widths with uniform air gap between the split membranes. This has helped to increase the mechanical resonant frequency and to minimize the effects of squeeze film damping. The membrane was subjected to modal analysis to estimate the resonant frequency so as to analyze the effect of vibrations when implemented in field

applications. The results are shown in the Table 3.2 for the six modes. The structural resonance of the first mode was found to be 16.84 KHz through the modal analysis. This value is quite satisfactory in response to the environmental effects this could face in the field applications. The natural frequency above 2000Hz ensures its reliable operation as per military standards.

TABLE 3.2: Modal Analysis for Resonance Frequency

Mode	**Frequency (KHz)**	**Mode Mass (kg.)**
1	16.84	6.95×10^{-10}
2	22.46	3.12×10^{-10}
3	37.38	3.31×10^{-10}
4	47.69	7.47×10^{-10}
5	50.13	3.80×10^{-10}
6	55.22	4.15×10^{-10}

The dynamic response was carried out using Intellisuite finite element analysis. The switching time can be computed by the equation (3). It has been observed that by keeping more gaps between the strips, membrane response time can be improved.

$$t_s \cong 3.67 \frac{V_p}{V_s} \frac{1}{2\pi f o} \tag{3}$$

Whereas V_p is the pull in voltage, V_s is the source voltage and f_o is the resonant frequency. From the simulation ON-time (downward transition) is 32µsec and OFF-time (upward) transition was found to be 48µsec as shown in the Fig. 3.11. A potential little over pull-in was applied to switch on the device.

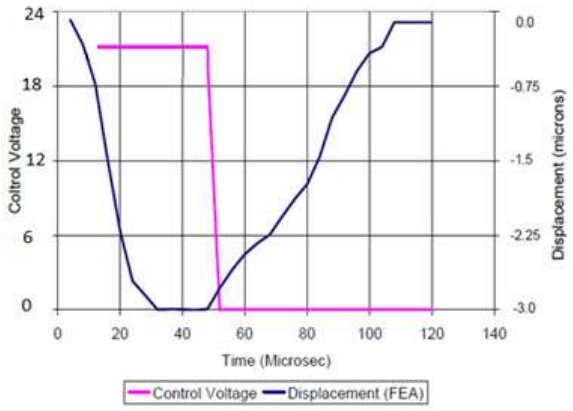


Fig. 3.11: Transition analysis for ON/ OFF time.

3.3 Layout Details

3.3.1 Double bias pad Configuration

Figure 3.12 (a) shows the detailed dimensions of the first metal layer layout. Figs. 3.12 (b), (c) and (d) show the details of tapered transition, bias pad and the DC line with gaps with respect to the ground.

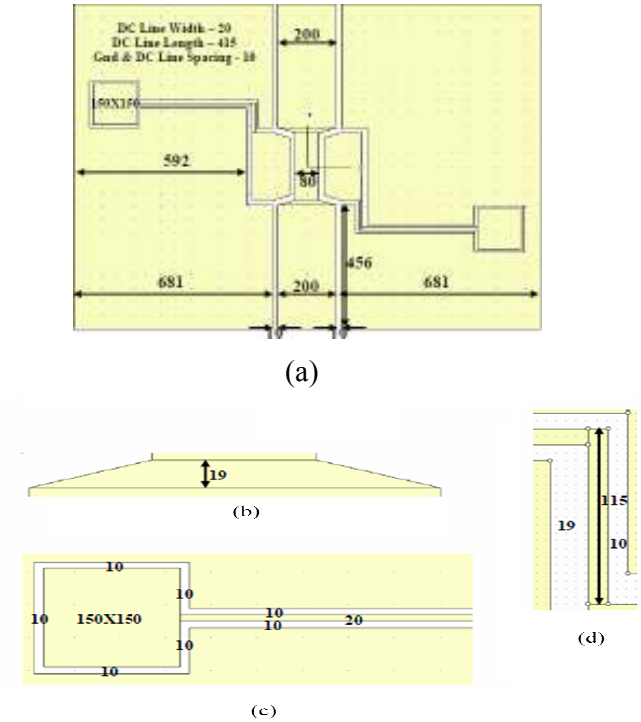
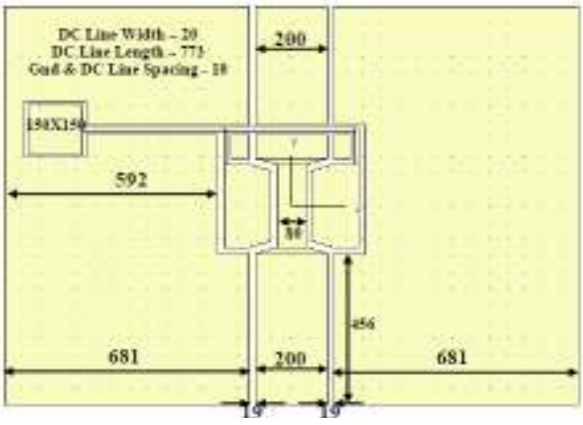


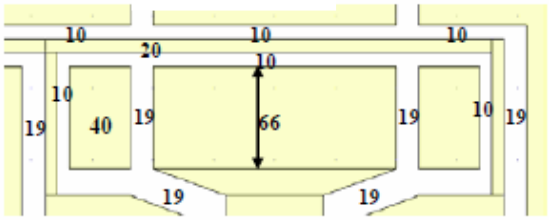
Fig. 3.12: (a) Full view with dimensions, (b) Tapering, (c) Bias pad and (d) DC Line.

3.3.2 Single bias pad Configuration

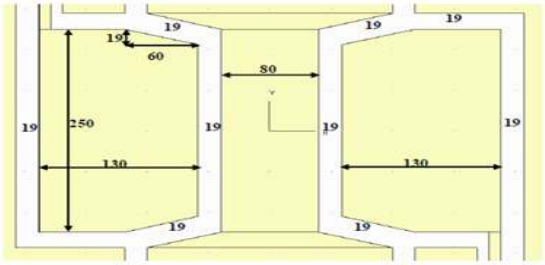
Figure 3.13 (a) shows the detailed dimensions of the first metal layer layout. The Figures 3.13 (b) shows the details of the RF line with DC bias pad with gaps with respect to the ground where as Figure 3.13 (c) shows the detailed dimensions of the electrodes which are common for both the configurations.



(a)



(b)



(c)

Fig. 3.13: (a) Full view with dimensions, (b) RF line with discontinuity for dc bias provision and (c) electrodes view with dimensions (common for both configurations).

3.4 Simulation Results

The Summary of simulation results for both capacitive type configurations are depicted in the Table 3.3. The simulation results in the frequency range of 4-20GHz have shown a small degradation in the insertion loss and return loss for the double DC bias pad in comparison to the single DC bias pad. The simulation and pull back voltage are same as the mechanical dimensions are exactly same for both the configurations.

Table 3.3: Simulation Results – Split Beam Capacitive Shunt Switch

Parameters	**Units**	**Single DC bias pad**		**Two DC bias pads**	
Frequency	[GHz]	**4-20**		**4-20**	
		Down State	UP State	Down State	UP State
Insertion Loss (S_{21})	[dB]	< - 40.10	> - 0.20	< - 42.8	> -0.15
Returns Loss (S_{11})	[dB]	> - 0.6	< - 26.0	< - 0.7	< - 29.2
Pull-in Voltage	[Volts]	≈ 22.2			
Pull back at	[Volts]	≈ 17.1			

3.5 Ohmic Series Configuration

The design of ohmic series switch was also done using split beams in rectangular shape instead of holes from other reported work. This configuration also in comparison to the rectangular holes has the advantage of low stress at the anchor junction, higher spring constant and higher mechanical resonant frequency making it more robust to the environmental effects and ease in structure release due to continuous larger gap for etchant percolation. Figure 3.14 (a) and (c) shows the 3D models of the split cantilever and rectangular holes analysed with FEM for stress analysis. The cantilever outer dimensions have been taken as same for both the configurations except for the internal structural design.

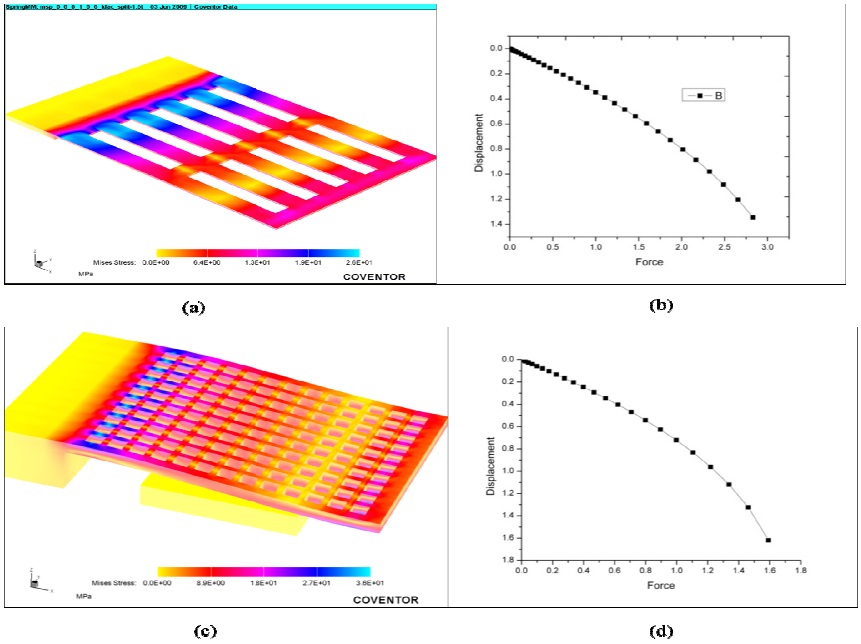


Fig. 3.14: (a) and (c) Stress analysis whereas (b) and (d) shows the force versus displacement curve for split and rectangular holes cantilever respectively.

The results show the low stress levels and higher linearity of the split cantilever configuration in comparison to the conventional rectangular holes concept. The units of the displacement and force shown are in µm and µN. The mass of the cantilever structure has

been maintained same for both the configurations so as to analyse the proposed split structure with respect to the rectangular holes structure. The holes dimension is 10x10 μm^2 and the edge to edge gap between the holes has been optimized in order to achieve the same mass as of the split beam structure. The split cantilever details are given subsequently. The analysis shows that the stress of the order 36 MPa in case of rectangular holes and 26 MPa for the split beam configuration has been observed. The stress analysis shows the superiority of split cantilever design with respect to the rectangular holes.

Figure 3.15(b) and (d) shows the force versus displacement graphs for these two configurations redrawn from the displacement versus voltage data of the CoventorWare finite element analysis using equation 4.

$$F = \frac{\varepsilon A V^2}{2g^2} \tag{4}$$

Where A = Area of electrode

g = gap between electrodes, 2.9 μm

ε = permittivity of air

V = applied voltage

The spring constant was derived using the slope of force versus displacement graphs at different points in the linear region using equation (5). The derived values of k have been found to be 2.86 N/m and 1.39 N/m for split beam and rectangular holes respectively clearly showing the advantage of split beam configuration in terms of superior spring constant.

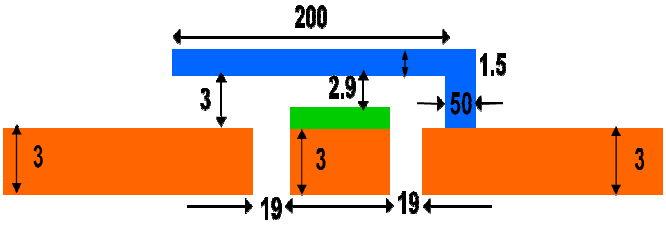
$$F = k\delta x \tag{5}$$

Where k = Stiffness

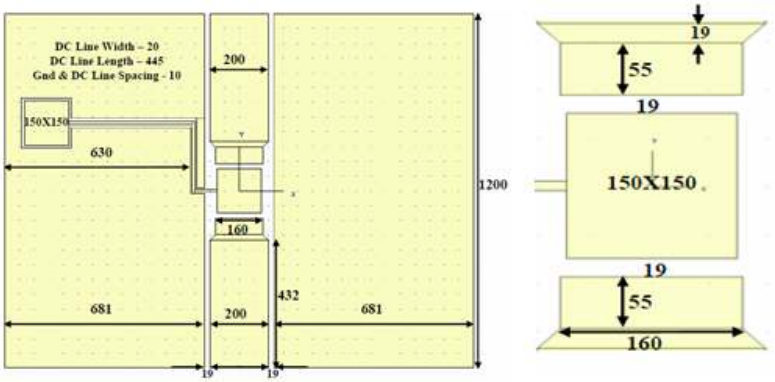
x = displacement

The above analysis clearly demonstrates the superiority of the split beam cantilever structure to the rectangular holes in terms of numerous parameters responsible for realization and the stable operation. Figure 3.15 (a) shows the cross sectional view of the ohmic series

having cantilever. The CPW of 50Ω impedance with Ground/Signal/Ground (GSG) configuration was used for design. The G/S/G dimensions for the CPW configuration are 19/200/19 µm. The air gap of 3.0µm was maintained for this design also, so as to process these in the same mask having same fabrication process. The actuation electrode was provided with the Si_3N_4 dielectric which makes this configuration less prone to stiction issues arising due to micro welding effects [101]. The CPW metal thickness was taken as 3.0µm for this design. In this structure, the 3D full wave electromagnetic simulation was carried out by a finite element method using Ansoft HFSS. The EM simulation results of RF parameters are shown in comparison to the measured results in the experimental results and discussion section. The cantilever was split into six strips each having width of 15µm and gap of 12µm.



(a)



(b) (c)

Fig. 3.15: (a) Cross section for cantilever having actuation electrode, (b) and (c) shows the details of the first metal layer and of the actuation electrode respectively. All dimensions shown in figures are in µm.

This was done keeping in view minimizing the effects of air damping and the easy removal of the sacrificial layer during the fabrication of MEMS switches. The pull in voltage was calculated using equation (1). Spring constant has been calculated using equation (6)

$$k = \frac{2\left(\frac{E}{1-v^2}\right)wt^3}{3l^3} \tag{6}$$

Where t = Thickness of membrane = 1.5 μm

E = Young's Modulus = 79 GPa

W= width of the beam

v = poisson's ratio

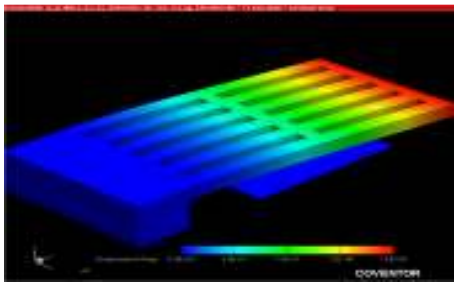


Fig. 3.16: 3D model of Cantilever under pull in analysis.

A 3D view of the cantilever under electrostatic simulation is shown in the Fig. 3.16 displaying maximum deflection at the edge of the cantilever. Based on the model values used in equation (6), the spring constant was found to be 4.04 N/m for the cantilever. These values were used in equation (1) and the pull in voltage was calculated as 12.53V. By simulation the pull in voltage is found to be 15.8V. Beyond the pull in voltage point a sudden snap down was observed and analyzed under contact and hysteresis analysis. The cantilever was analyzed for the hysteresis response which is quite crucial for the smooth operation of the switch. Figure 3.17 shows the contact analysis and hysteresis curve after removal of the DC bias from the actuation electrodes and the cantilever comes back to its original position under force of spring constant at 12.6V for air gap of 3.0μm. The simulations were carried out using

FEM model of the switch. The hysteresis curve shows the pull back of the cantilever after removal of the actuation voltage.

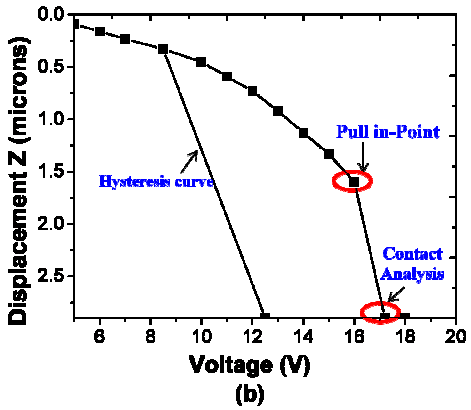


Fig. 3.17: Contact Analysis and Hysteresis curve.

The cantilever was subjected to modal analysis using CoventorWare to estimate the resonant frequency so as to analyze the effects of various vibrations when implemented in field applications. Keeping in view the effect of split beam the damping was considered zero during simulation. The structural resonance frequency was found to be 11.199 KHz. The value is quite satisfactory in response to the environmental effects this could face in the field applications. Table 3.4 shows the values of the resonance frequency of the first six modes.

Table 3.4: Modal Analysis frequency for Cantilever

Mode	Frequency (KHz)	Mass (kg.)
1	11.199	1.73×10^{-11}
2	41.908	1.10×10^{-11}
3	64.125	1.93×10^{-11}
4	132.803	9.60×10^{-12}
5	141.402	1.04×10^{-11}
6	185.063	2.14×10^{-11}

The dynamic response of the switch was carried out using Intellisuite finite element analysis. The cantilever was split into smaller width with air gap in between the strips to improve the time response of the switch. The switching time can be computed by the equation (8). It has been observed that by keeping more gap between the strips time response can be improved. Whereas V_p is the pull in voltage, V_s is the source voltage and f_o is the resonant frequency. From the simulation ON-time (downward transition) is 21 µsec and OFF-time (upward) transition was found to be 19µsec for the switch as shown in the Fig.3.18. A potential of 21.0V was applied to switch on the device.

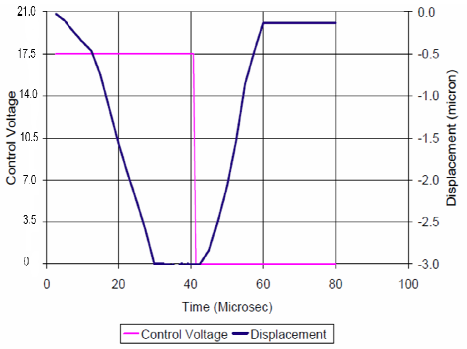


Fig. 3.18: Switch Transition analysis for on / off time.

3.5.1 Simulation Results

The simulation shows the insertion loss as 0.15dB and return loss better than 22.7dB for this configuration at 17.1V of pull in voltage.

Table 3.5: Summary Simulation Results – Ohmic Series Switch

Parameters	**Units**	**Split beam Cantilever**	
Frequency	[GHz]	DC – 12 GHz	
		ON State	OFF State
Insertion Loss (S_{21})	[dB]	< - 0.15	< - 45.2
Returns Loss (S_{11})	[dB]	> - 22.7	< - 0.5
Pull-in Voltage	[Volts]	≈ 17.1	
Pull back at	[Volts]	≈ 13.4	

Summary

This chapter has presented the concept of split beam for capacitive shunt and for the ohmic series RF MEMS switches. Both the configurations have been compared and analyzed against the rectangular hole type configurations very commonly observed in the literature. The proposed design of split configuration has shown its superiority with respect to rectangular holes type in terms of spring constant and low stress levels during simulation analysis. Single DC bias pad configuration of the capacitive shunt switch has also shown very negligible degradation in the insertion and the return loss in the EM simulations. This configuration has lot of ease in system implementation due to its simple layout.

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CHAPTER 4

MEMS SWITCH FABRICATION, INSPECTION & RF MEASUREMENT

The fabrication of MEMS devices is the one the critical areas. Surface micromachining has been the established technique for fabrication of the RF MEMS. The aim of this chapter is to present the fabrication details along with the in depth inspection procedures adopted during the various stages and after the completion of the device fabrication to verify the significant parameters. DC and RF measurements are also presented which confirms the development of the switches meeting all electrical requirements.

4.1 Process Flow

The fabrication of the switches was carried out using surface micromachining techniques. Process was customized according to the design requirements. A four mask batch process was used to fabricate the micromechanical switches. The cross-sectional fabrication flow is shown in Fig. 4.1 (a-f). Quartz was chosen for fabrication as the substrate plays an important role in determining the electrical performance of the RF MEMS switches at microwave frequencies. In addition, it has better temperature stability at high temperatures. The quartz substrate of 525 μm thickness with 4 inch diameter was taken for fabrication. The first metal (Au) of 3.0μm thickness for CPW was deposited through E-beam evaporation and patterned as shown in Fig. 4.1 (b) using mask 1. In order to avoid metal-metal contact a Si_3N_4 (Silicon nitride) layer of 0.1μm was deposited using PECVD and patterned over the transmission line and the actuation pads as shown in Fig. 4.1 (c) using mask 2. The 3.5μm of

photo resist above the CPW metal was coated using spin coating in two steps. A novel technique of photo resist planarization was implemented to avoid the beam deposition on uneven surface.

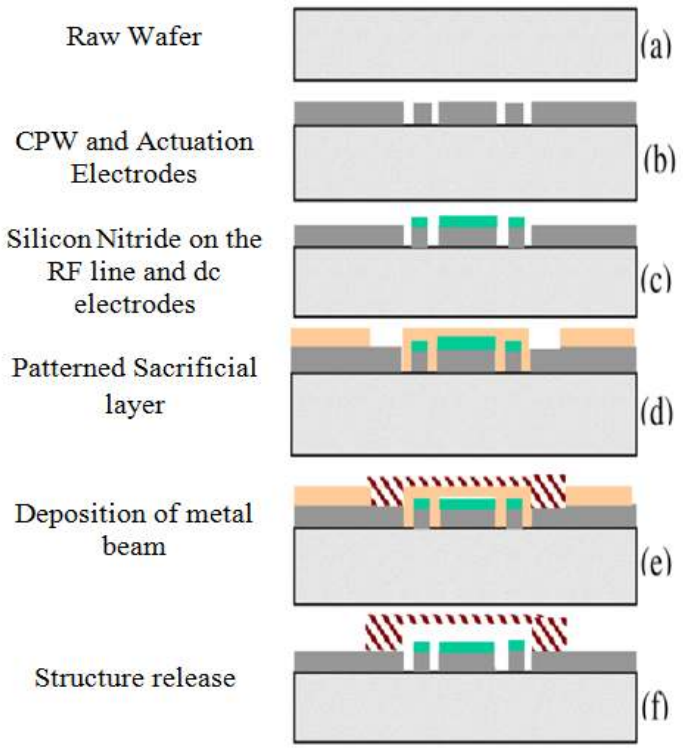


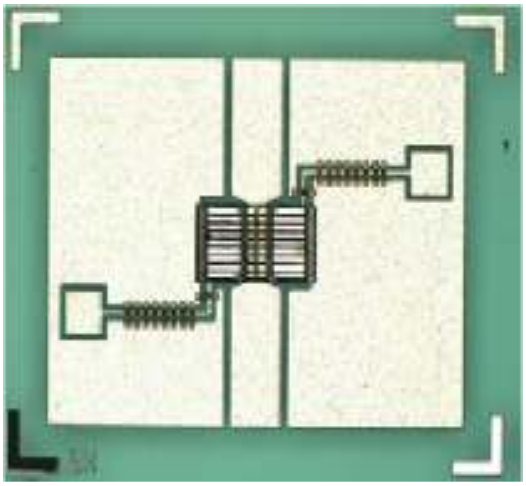
Fig. 4.1: (a) to (f) Cross section of fabrication flow followed during the switch fabrication.

The photo resist coating was done in two steps with a optimized speed. The layer was coated using low speed for filling and the second coating was performed a higher speed to attain the planarized surface for the beam deposition. Mask 3 was used for opening through the sacrificial layer for the beam anchor. The opening is shown in the sacrificial layer in Fig. 4.1 (d). The beam structure with 1.5µm thickness was realized through RF sputter deposition in Fig. 4.1 (e). At the last sacrificial layer was ashed out using plasma etching and release of the switch is shown in the Fig.4.1 (f). Both configurations namely single and double dc bias pas were fabricated in the same mask using the same fabrication process.

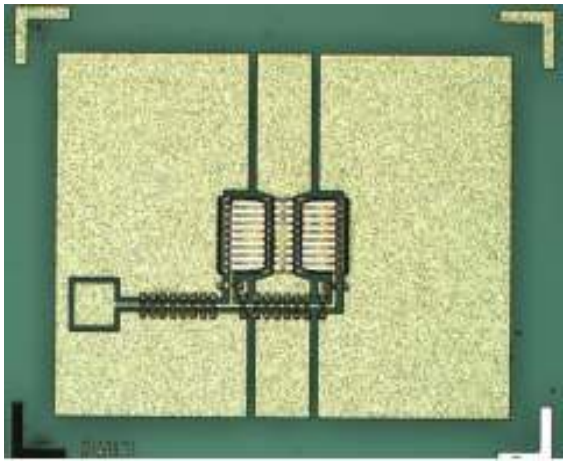
4.2 Inspection

4.2.1 Optical Inspection

The optical inspection was carried out using Olympus STM series microscope. The optical image of the double bias pads and single bias configuration is shown in the Figure 4.2 (a) and (b) respectively.



(a)



(b)

Fig. 4.2: Optical view of the fabricated (a) double dc bias pad and (b) single dc bias pad configuration.

4.2.2 Air gap measurement

The performance of the switch is significantly dependent on the air gap between the membrane and the electrodes. The ratio of the up and down state capacitance is proportional

to the distance between the two states. The accurate measurement is essential to inspect the fabricated structure with respect to the design so the air gap measurement for double DC bias pad was carried out by non contact methodology using sophisticated instrument namely laser vibrometer under the surface topography mode. The measured device is shown in the Fig. 4.3. This was scanned also across the membrane and it shows the individual step height of the beam. The results were observed in line to the design and fabrication. Membranes were found to be having the air gap as 2.88µm.

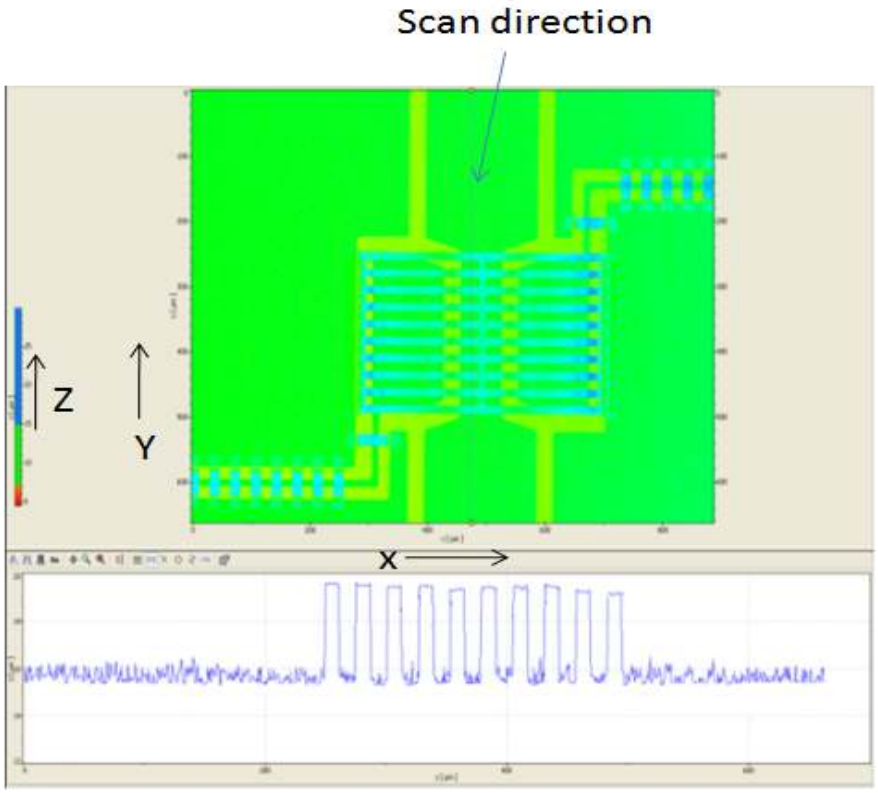
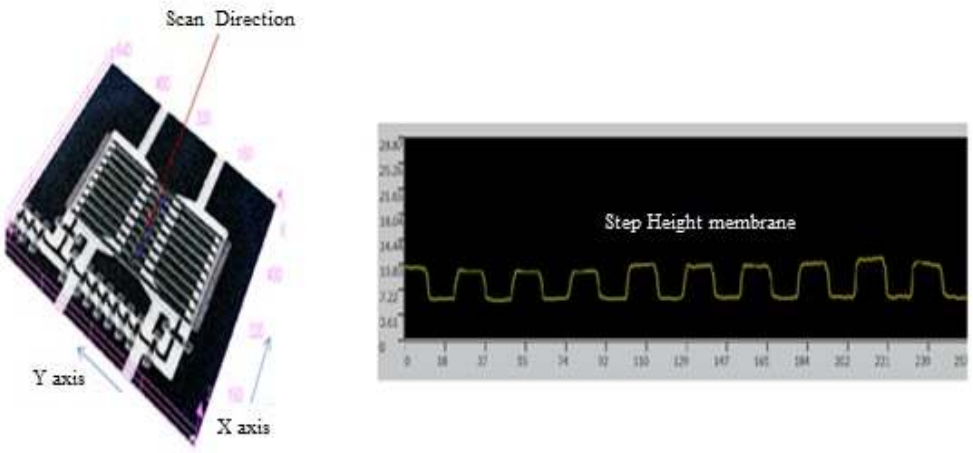


Fig. 4.3: Air gap measurement of beam from the bottom electrode in non contact mode using the laser vibrometer. The cantilever was scanned across the length so as to confirm the planarity. X and Y axis shows the width and length respectively. Z axis shows the gap height of the membrane from the bottom electrode.

However for single DC bias pad configuration LEXT OLS 3100 confocal laser scanning microscope was used for air gap measurement. The measured device is shown in the

Fig. 4.4(a). This was scanned across the width of the membrane and it shows the individual step height of the split beam. X and Y axis shows the width and length respectively. This scan direction gives the results about all the beams as even one beam not in same plane could make the switch non functional. Figure 4.4(b) shows the graph after measurement of the fabricated single bias pad configuration. The results were observed in consonance to the design and fabrication.

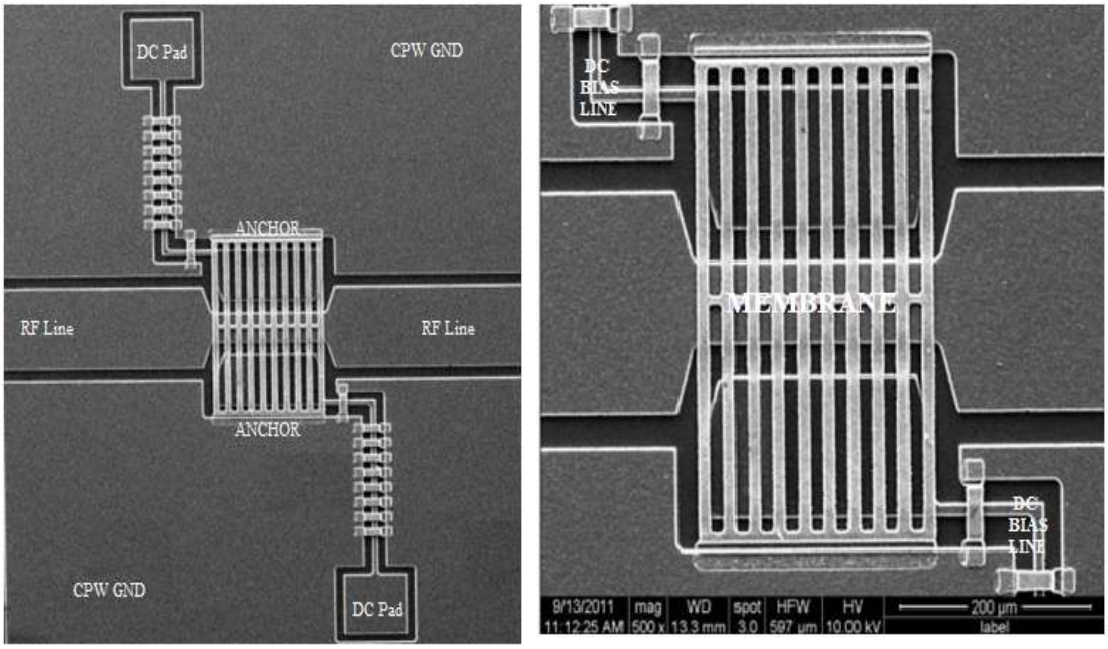


(a) (b)

Fig.4.4: (a) Scan direction and (b) air gap was observed as 2.84 μm from the top surface of the bottom electrode as against the Z axis.

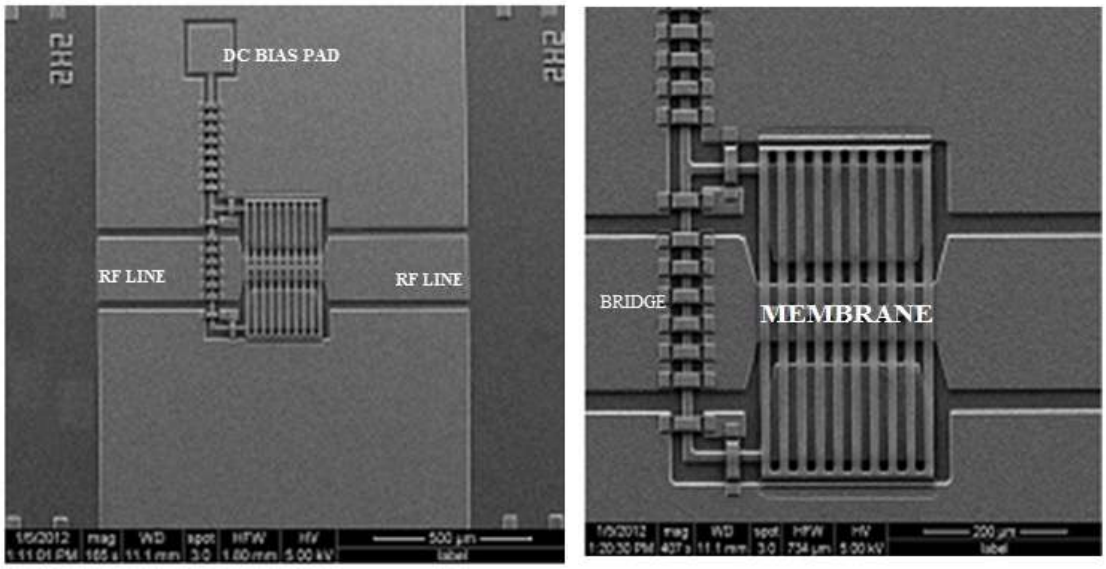
4.2.3 Surface Topography Inspection

In order to inspect and analyze the surface topology of the fabricated device SEM inspection was carried out. Figure 4.5 (a) shows the surface view of the complete device while Fig. 4.5 (b) shows the zoomed SEM view of the membrane area of double DC bias configuration. Figure 4.6 (a) and 4.6 (b) shows the single DC bias pad configuration. This analysis has given clear view of the edge definition and interspacing of the split membranes. SEM inspection also revealed the complete removal of the sacrificial layer enabling the device to properly perform electrically during the deflected state.



(a) (b)

Fig.4.5: (a) SEM view of the full device and (b) Zoomed view of the membrane area of double dc bias pad.



(a) (b)

Fig.4.6: (a) SEM view of the full device and (b) Zoomed view of the membrane area of single dc bias pad.

4.3 Experimental Results and Discussions

4.3.1 DC Characteristics

C_{up} and C_{down} i.e. Capacitance in upstate and deflected state was measured at 1MHz using the semiconductor parametric analyzer B1500 of the Agilent. The complete test set up is shown in the Fig. 4.7. The capacitance ratio (C_{down}/C_{up}) had been measured in the range of 30-35. The absolute values of measurement are shown in the Table 4.1.

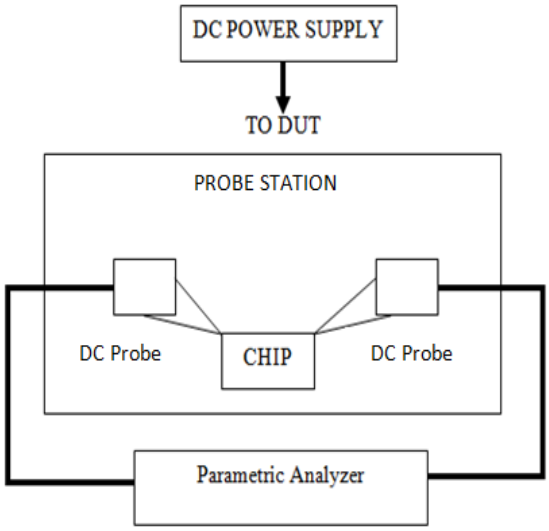


Fig. 4.7: Test set up for measurement of capacitance

4.3.2 RF Characteristics

Two port on wafer RF measurements for the 'S' parameters were carried out from 4-20 GHz. The semi-automatic RF probe station of Cascade Microtech Summit 11000 series with Vector Network Analyzer E8363B of Agilent make was used to characterize the switch device. The short open load thru (SOLT) technique was used to calibrate the test set up. A separate standard impedance substrate was used for calibration. The measurement accuracy is traceable to international standards.

4.3.2.1 Double DC Bias Pad

Figure 4.8 shows the switch measurement view which has double dc bias electrodes on both sides having symmetrical pull in arrangement. The S parameter measurement of the switch has insertion loss of 0.20 dB and return loss better than 24 dB in upstate from 4-20 GHz as shown in fig. 4.9(a). In the down state switch has isolation better than 40 dB as shown in the Fig. 4.9(b).

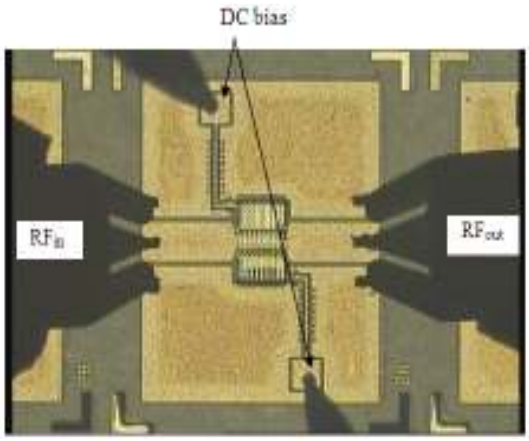
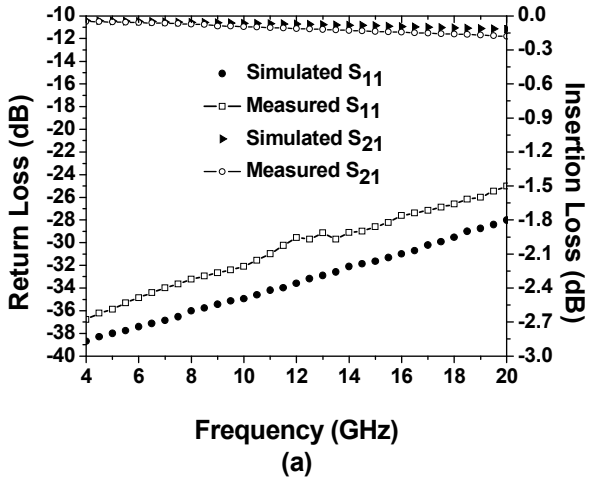


Fig. 4.8: Fabricated switch measurement set up for the CPW (GSG) configuration measured with 200 micron pitch probe for double dc bias.



(a)

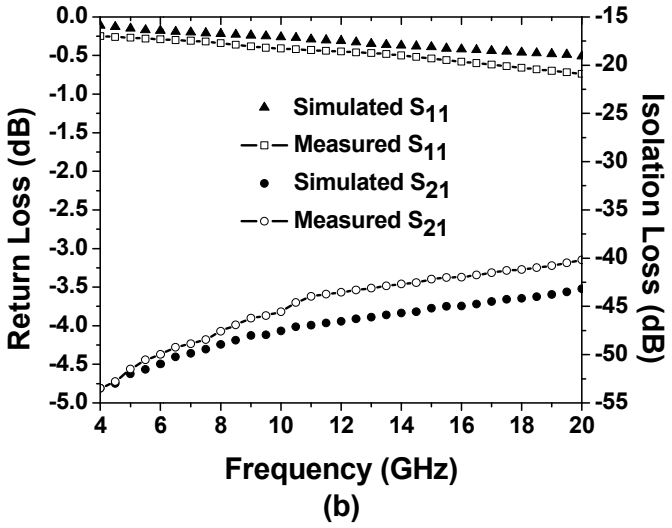


Fig. 4.9: S parameter measured results (a) upstate of the switch, return and insertion loss (ON state) and (b) downstate of the switch, isolation are compared against the simulated results (OFF state).

4.3.2.2 Single DC Bias Pad

Fig. 4.10 shows the switch measurement view which has single dc bias pad for both sides of symmetrical pull in electrodes.

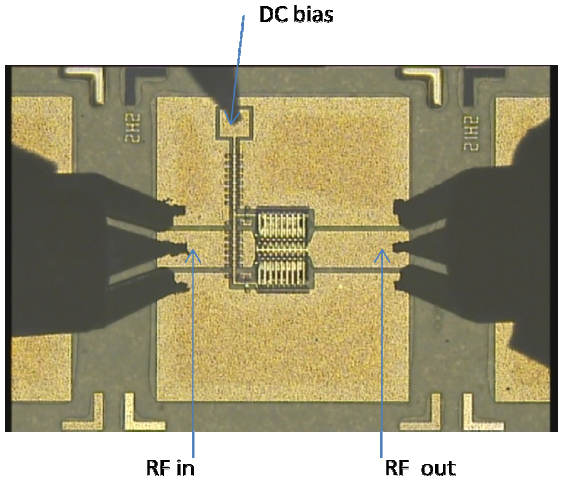


Fig.10: Fabricated switch measurement set up showing the single bias pad configuration measured with 200 micron pitch probe.

The S parameter measurement of the switch has shown insertion loss of 0.24dB and return loss better than 22dB in upstate from 4-20 GHz as shown in Fig. 4.11(a). In the down state switch has isolation better than 37 dB as shown in the Fig. 4.11(b).

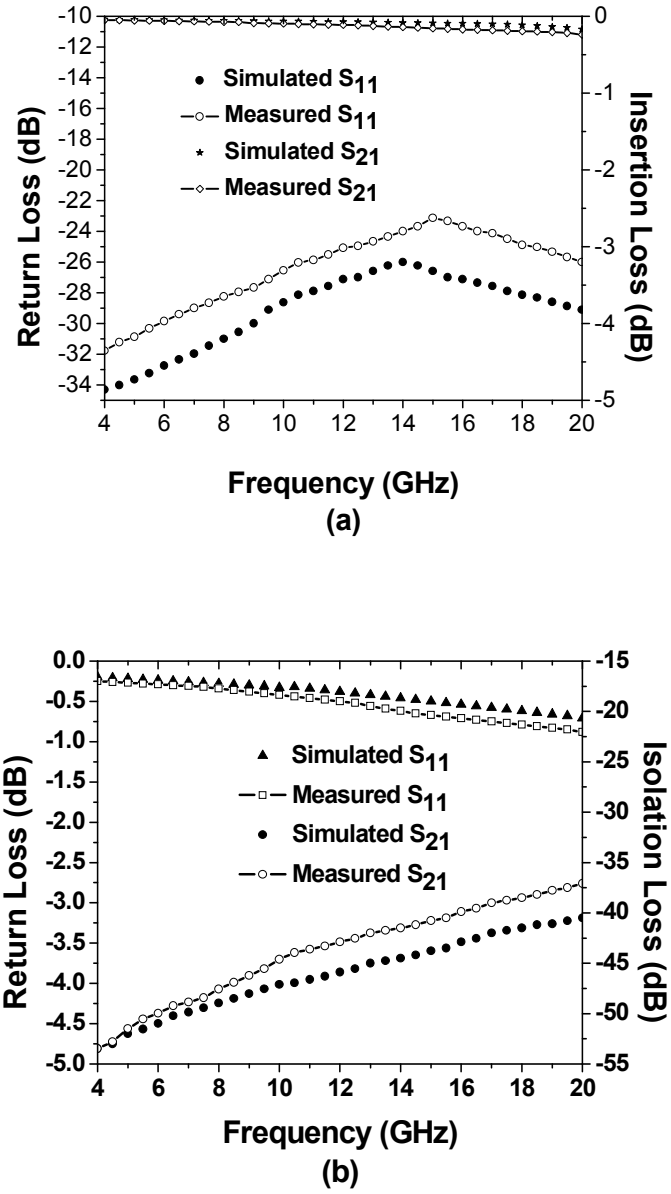


Fig. 4.11: S parameter measured results (a) upstate of the switch, return and insertion loss (ON state) and (b) downstate of the switch, isolation are compared against the simulated results (OFF state).

The parameters of the designed, simulated, fabricated and measured capacitive shunt configurations are presented in Table 4.1.

Table 4.1: Summary of Parameters for the Developed Shunt Switch

Parameter	**Value**	**Parameter**	**Value**	
Length[μm]	396	Sacrificial layer	Photoresist	
Width[μm]	249	Beam Type	Split beams	
Height [μm]	2.84(measured)	Dielectric(Å)	1000	
Membrane Layer	Au	Actuation area[μm^2]	250x130 (x2)	
Thickness [μm]	1.5	Actuation voltage[V] (measured)	24.6	
Spring Constant[N/M] (Calculated value)	17.17	Switch time[μs] (simulated)	30-50	
Effective mass [Kg]	18.557×10^{-10}	C_u[fF] (measured)	231.5	
Density of Material [Kg/m^3]	19,320	C_d[pF] (measured)	6.96	
		Return Loss[dB] (measured)	Single bias -22.0	Double bias -24.0
Mechanical Resonance frequency [KHz]	15.31(calculated)	Insertion Loss[dB] (measured)	< -0.24	< -0.20
	16.84 (simulated)	Isolation[dB] (measured)	< -37.0	< - 40.0

4.4 Fabrication – Ohmic Series

The fabrication of the ohmic series switch was also carried out using surface micromachining techniques in the same mask of capacitive shunt switch. Process was customized according to the design requirements. The same four mask process was followed as explained in the shunt switch fabrication. The cross section is shown in the Fig. 4.12.

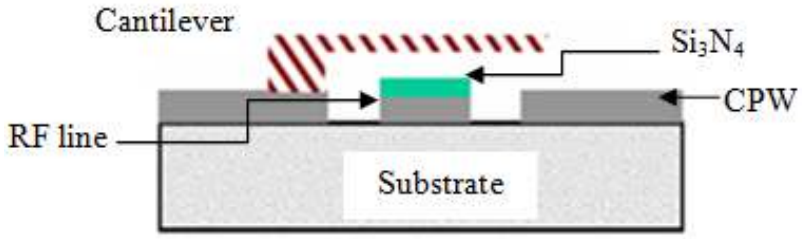


Fig. 4.12: Cross section of the ohmic series switch.

4.5 Inspection

4.5.1 Optical Inspection

The optical inspection was carried out using Olympus STM series optical microscope. The optical image of the ohmic series configuration is shown in the Fig. 4.13.

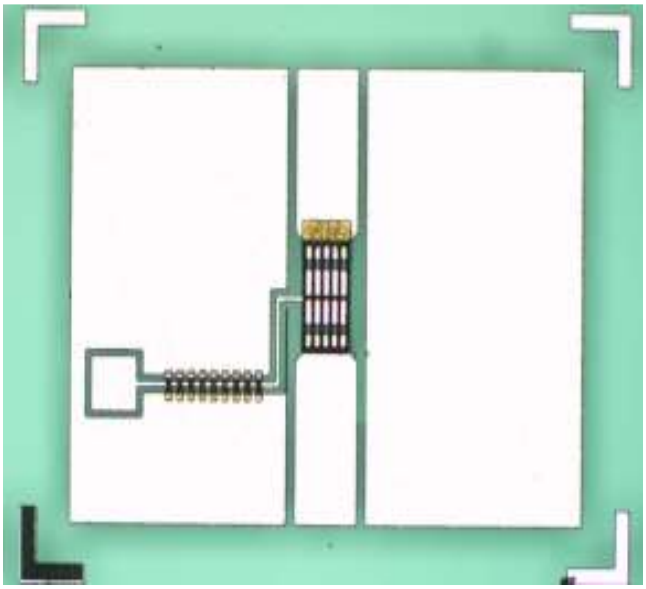


Fig. 4.13: Optical view of ohmic series configuration.

The optical image shows the series configuration has the cantilever in continuation to top of the RF line which provides RF continuity upon actuation. The bias pad on is connected through DC line and ground continuity has been provided via air bridges.

4.5.2 Air gap measurement

The air gap measurement was carried out by non contact methodology using laser vibrometer under the surface topography mode. The switch was scanned along the length and it shows the single step which also includes the thickness of the cantilever as shown in Fig. 4.14. The results were observed in agreement to the design and after fabrication were found to be having the air gap as 2.9μm.

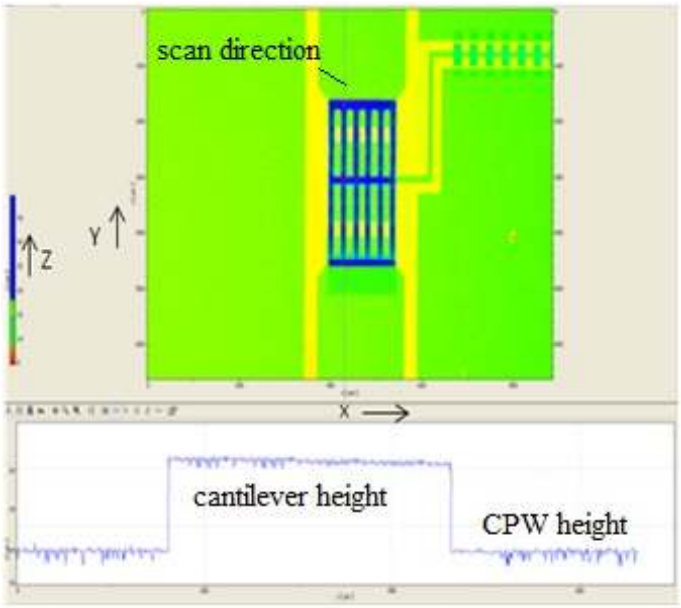
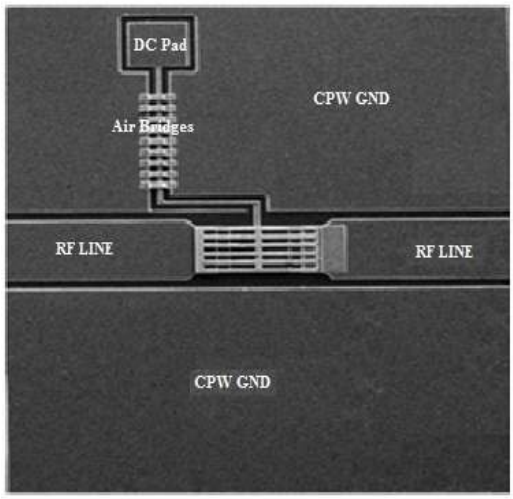


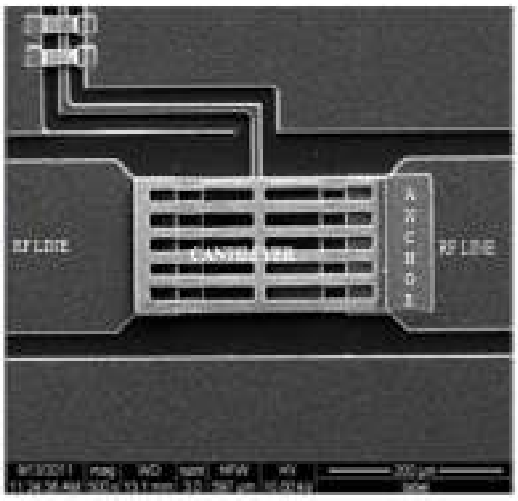
Fig. 4.14: Air gap measurement of cantilever from the bottom electrode in non contact mode using the laser vibrometer. The cantilever was scanned across the length so as to confirm the planarity. X and Y axis shows the width and length respectively. Z axis shows the gap height of the cantilever as 2.9 μm from the bottom electrode.

4.5.3 Surface Topography Inspection

SEM inspection was carried out to analyze the surface topology of the fabricated device. Figure 4.15 (a) shows the complete surface view and (b) the zoomed SEM view of the device. This analysis has given clear view of the edge definition and interspacing of the split membranes. SEM inspection also revealed the complete removal of the sacrificial layer enabling the device to properly perform electrically during the deflected state.



(a)



(b)

Fig. 4.15: (a) SEM view of the complete series switch and (b) Zoomed view of the Cantilever area.

4.6 Experimental Results and Discussion

4.6.1 DC Characteristics

C_{up} and C_{down} i.e. Capacitance in upstate and deflected state was measured at 1MHz using the parametric analyzer of the Agilent. The capacitance ratio (C_{down}/C_{up}) has been measured in the range of 30-35 for this configuration also.

4.6.2 RF Characteristics

The RF measurements for the 'S' parameters were carried out from DC-12 GHz. The similar set up as described for the shunt switch measurement has been used. Figure 4.16 shows the device setup for measurement.

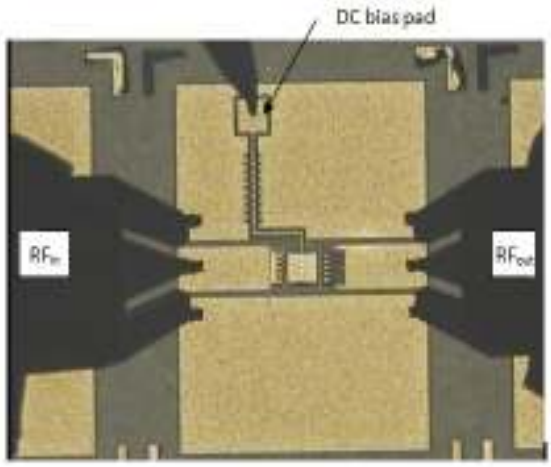
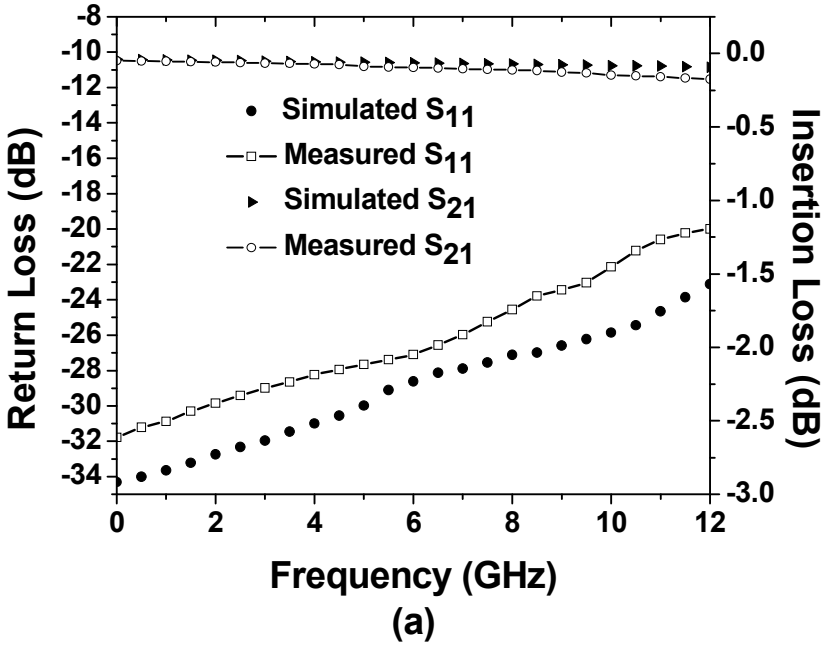


Fig. 4.16: Fabricated switch measurement view showing the series configuration

The S parameters are shown in the Fig. 4.17 (a) and (b) for the down and up state respectively. The insertion loss in on state is better than 0.18 dB with minimum return loss of 21dB from DC-12 GHz. The isolation is better than 40 dB. The RF measurement results indicate the series switch has good ohmic contact with RF line for low loss transmission of the signal. The measured parameters show a very good consonance with the simulated results.



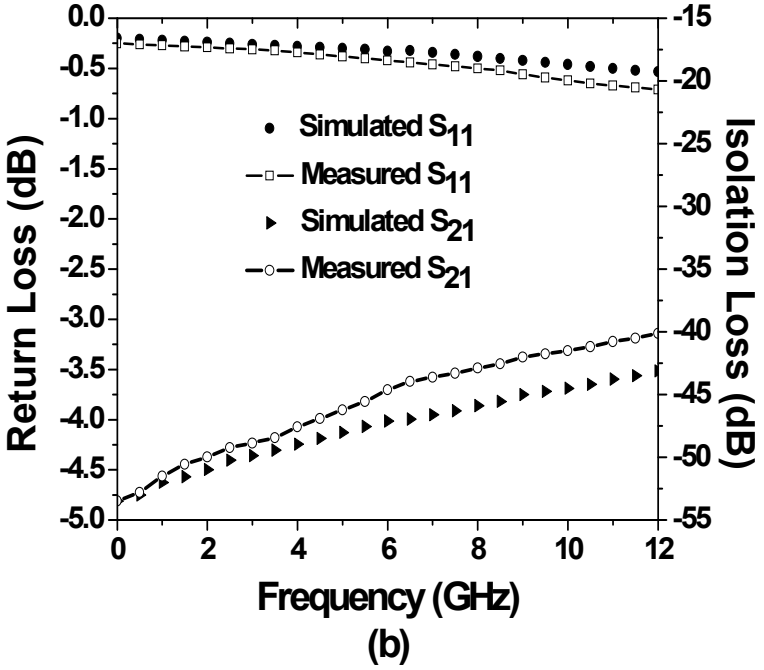


Fig. 4.17: S parameter measured results (a) downstate of the switch, return and insertion loss (ON state) and (b) upstate of the switch, isolation are compared against the simulated results (OFF state).

The parameters of the designed, simulated, fabricated and measured Ohmic switch are listed in Table 4.2.

Table 4.2: Summary of Parameters for the Developed Ohmic Series Switch

Parameter	**Value**	**Parameter**	**Value**
Length[μm]	200	Sacrificial layer	Photo resist
Width[μm]	150	Membrane Type	Cantilever
Height [μm]	2.9 (measured)	Dielectric(Å)	1000 (on actuation pad)
Membrane Layer	Au	Actuation area[μm^2]	140x150
Thickness [μm]	1.5	Actuation voltage[V] (measured)	18.1
Spring Constant[N/M] (Calculated value)	4.04	Switch time[μs] (simulated)	15-25
Effective mass [Kg]	8.69×10^{-10}	C_u[fF] (measured)	168.0
Density of Material [Kg/m^3]	19,320	C_d[pF] (measured)	5.59
Mechanical Resonance frequency [KHz]	10.85 Calculated	Loss[dB] (measured)	0.18
	11.19 simulated	Isolation[dB] (measured)	> 40

SUMMARY

This chapter has presented the complete details of the fabrication, inspection with dc & RF characterization of both the configurations namely capacitive shunt and ohmic series. Capacitive shunt in turn had two variables with single and two dc bias pads. It has been

observed that single bias pad shunt switch has shown a negligible degradation in the insertion loss. It can be concluded that single dc pad switch can be preferred over two dc bias pads due to its comparable RF performance but having a considerable ease in system implementation. The capacitive switches have been optimized from 4-20GHz frequency range. Ohmic series switch has also shown RF performance in consonance with the simulation results. The ohmic switch has been characterized from DC-12GHz. The performance of both type of switches make them suitable for the circuit level implementation. These can be employed in phase shifters and reconfigurable circuits.

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CHAPTER 5

Design & Simulation of 5-bit Ku band Phase Shifter

The analog and digital are the two basic types of phase shifters. The analog phase shifter results in a continuously variable phase shift from 0° to 360° and is designed using varactors. Digital phase shifters provide a discrete set of phase delays and are usually built using switches. For example, principal bits in a 4-bit phase shifter are 22.5°/45°/90°/180°. By using a set of delay networks one can achieve the phase shifts of 0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, 157.5°, 180°, 202.5°, 225°,247.5°,270°,292.5°,315° and 337.5°. The scanning resolution and side lobe levels of a phased array antenna are directly related to the number of bits employed. Most systems require a 3-bit or a 4-bit phase shifter but high performance systems in defense and space require 5 or 6-bit MEMS phase shifters. The MEMS based phase shifters can be designed with various topologies based on different switch configurations. This chapter presents the design and RF simulation of the ohmic series switch constituting phase shifter, single and 5-bit integrated phase shifter configuration. Layout details and analysis of the MEMS structures is described for pull in voltage and tip bending versus stress gradient. This chapter also covers the 5-bit phase shifter design on GaAs.

5.1 Phase Shifter Design

In view of the unavailability of the standardised process RF MEMS foundry in India, it was needed to explore and use the foreign foundry having an established fabrication line. Based on the survey the Fondazione Bruno Kessler (FBK) Italy was selected for fabrication and the design was tuned according to the process inputs from the foundry.

The phase shifter topology is optimized using hybrid architecture, which consists of the combination of switched line and loaded line topologies. The first three bits namely 180°, 90° and 45° were realized by switched microstrip lines using ohmic MEMS switches in series mode, whereas the 4^{th} and 5^{th} bits namely 22.5° and 11.25° consist of microstrip line sections loaded by ohmic series switch in shunt mode. The switched line was adopted for larger bits as it provides higher phase accuracy. The loaded line topology is preferable for smaller phase bits as these do not need higher loading and also it is less sensitive to variations of the contact resistance. High Resistivity Silicon (ε_r=11.7, thickness=200±10μm) was identified as the substrate since it provides higher Δ_φ/mm and Δ_φ/dB leading to high compactness and low loss. This topology indeed seems to be the best trade-off among large phase shift, low loss and reduced space occupation in the selected frequency band. Both CPW and microstrip configurations have been designed for phase shifter. Microstrip configuration was chosen to implement in system in view of its compatibility to interface with other devices. Moreover it provides lower loss and enhanced compactness with respect to CPW. Ohmic series MEMS cantilever switches have been used as switching elements of the proposed phase shifter. The detailed design has been carried out using full wave electromagnetic simulators ADS Momentum and Ansoft HFSS. Simplified structures of single bits have been drawn in the simulation layout, in order to reduce the computation time and to increase the simulation accuracy.

5.2 RF Results of Ohmic Series Switch Constituting Phase Shifter

The layout of the ohmic series switch is presented in Fig. 5.1(a). It consists of a gold membrane of 110μm width and 170μm length suspended above an interrupted transmission line and anchored at one end called cantilever. In the off state it provides very high wide-band isolation from DC up to high frequencies. In the on state the bridge is pulled down by electrostatic forces produced by the voltage applied to the actuation pad and contacts the

interrupted signal line. The simulated RF performance of the ohmic series switch is shown in Fig. 5.1(b). It shows isolation better than 23 dB and an insertion loss better than 0.2 dB up to 20 GHz frequency range. These values correspond to an off-state capacitance of 10 fF and an on-state resistance of 0.9 Ohm. The dielectric on top of the fixed electrodes of the MEMS switch was removed in order to mitigate the dielectric charging phenomena.

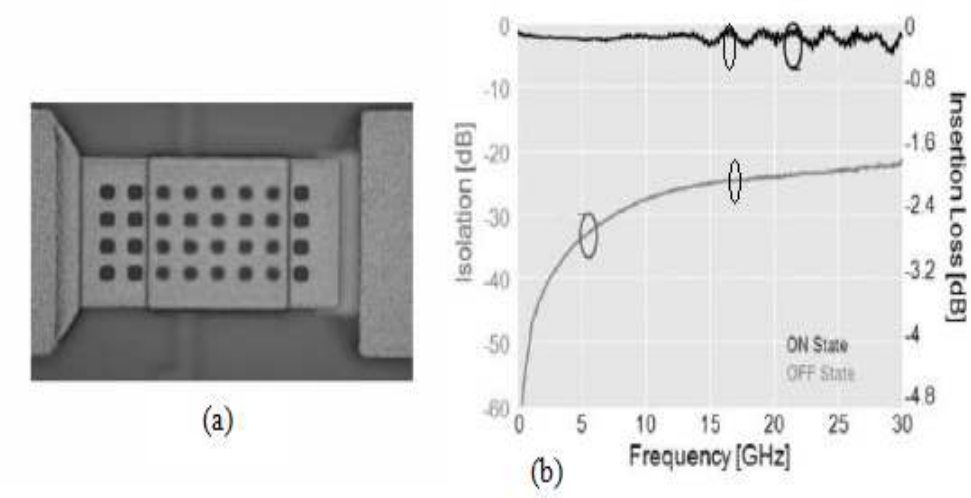


Fig. 5.1: (a) Layout and (b) expected performance of the MEMS SPST cantilever switch constituting the phase shifter.

5.3 Simulation Results of Single bits

The individual bits have been designed and simulated to ensure the desired performance of the 5-bit integrated phase shifter. By employing the switch shown in Fig. 5.1, individual bits and integrated 5-bit MEMS phase shifter (CPW and microstrip) in the 16-18 GHz frequency range has been designed using ADS momentum. The layout and simulated performance of the individual bits are shown in the Fig. 5.2 to 5.6. The geometry of every single bit has been optimized in order to minimize the insertion loss as well as moving out of band the ring resonances due the non-zero off-state capacitance of the MEMS switches.

Figure 5.2 (a-d) shows the layout and 180^0 bit simulation results for short and long path i.e. reference and delay path. The bit 1 has shown insertion and return loss better than 0.38dB and 19dB respectively in 16-18 GHz frequency band.

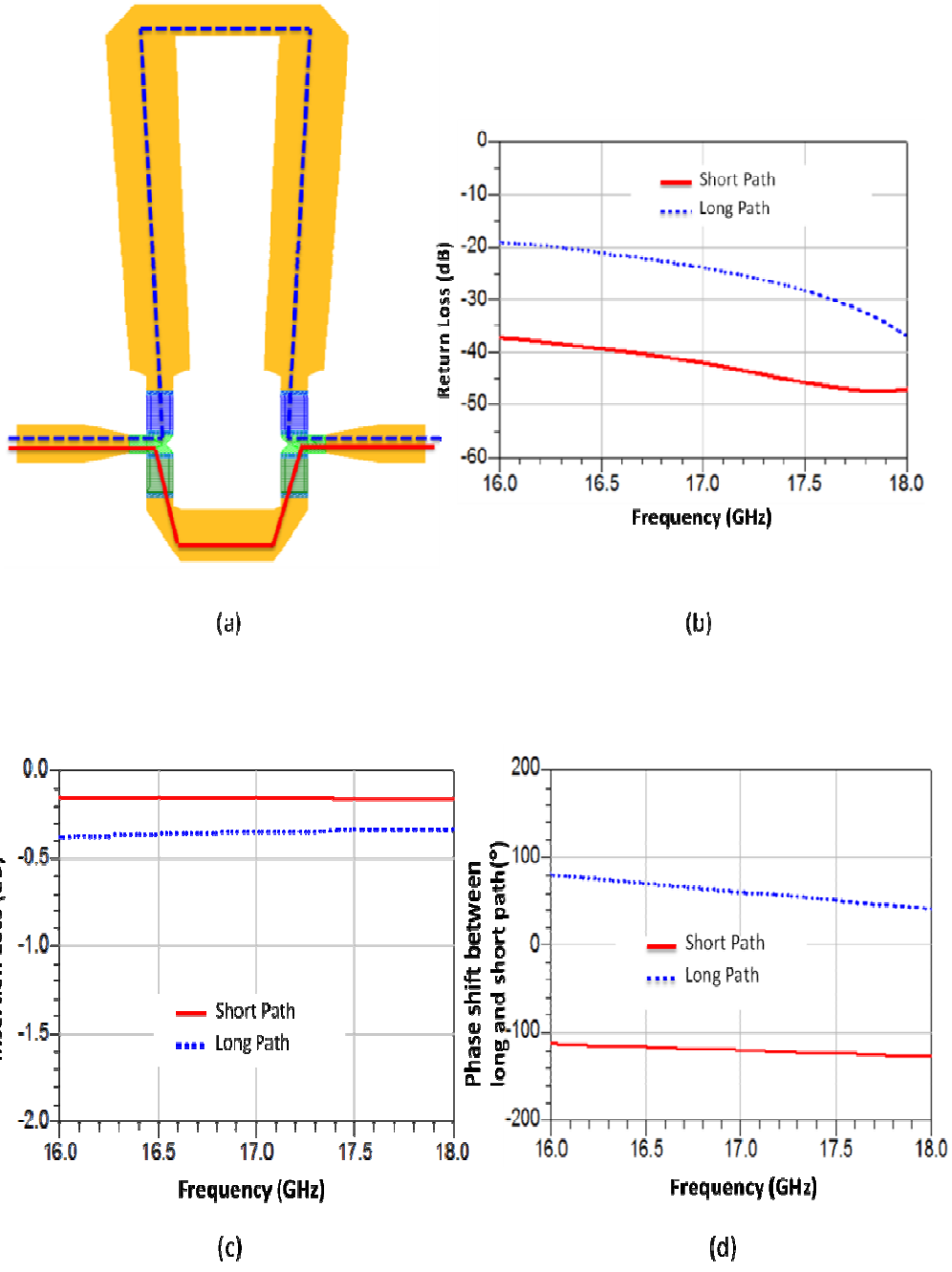


Fig.5.2: (a) Layout, (b) simulated return loss, (c) insertion loss and (d) phase shift of the 180^0 bit '1'.

Figure 5.3 (a-d) shows the layout and 90° bit simulation results for short and long path i.e. reference and delay path. The bit 2 has shown insertion and return loss better than 0.45dB and 29dB respectively in 16-18 GHz frequency band.

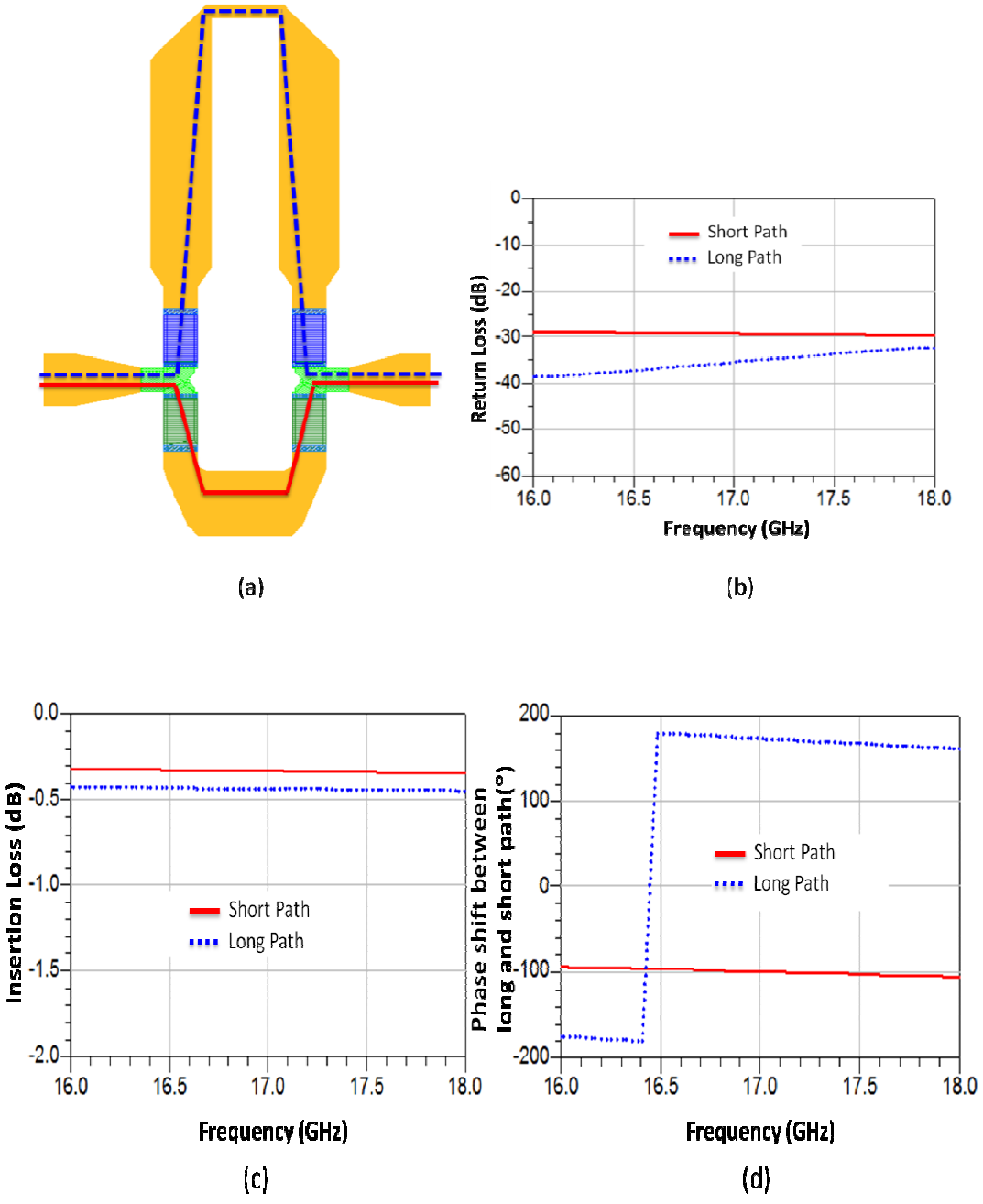


Fig.5.3: (a) Layout (b) simulated return loss (c) insertion loss and (d) phase shift of the 90^0 bit '2'.

Figure 5.4 (a-d) shows the layout and 45° bit simulation results for short and long path i.e. reference and delay path. The bit 3 has achieved insertion and return loss better than 0.28dB and 26dB respectively in 16-18 GHz frequency band.

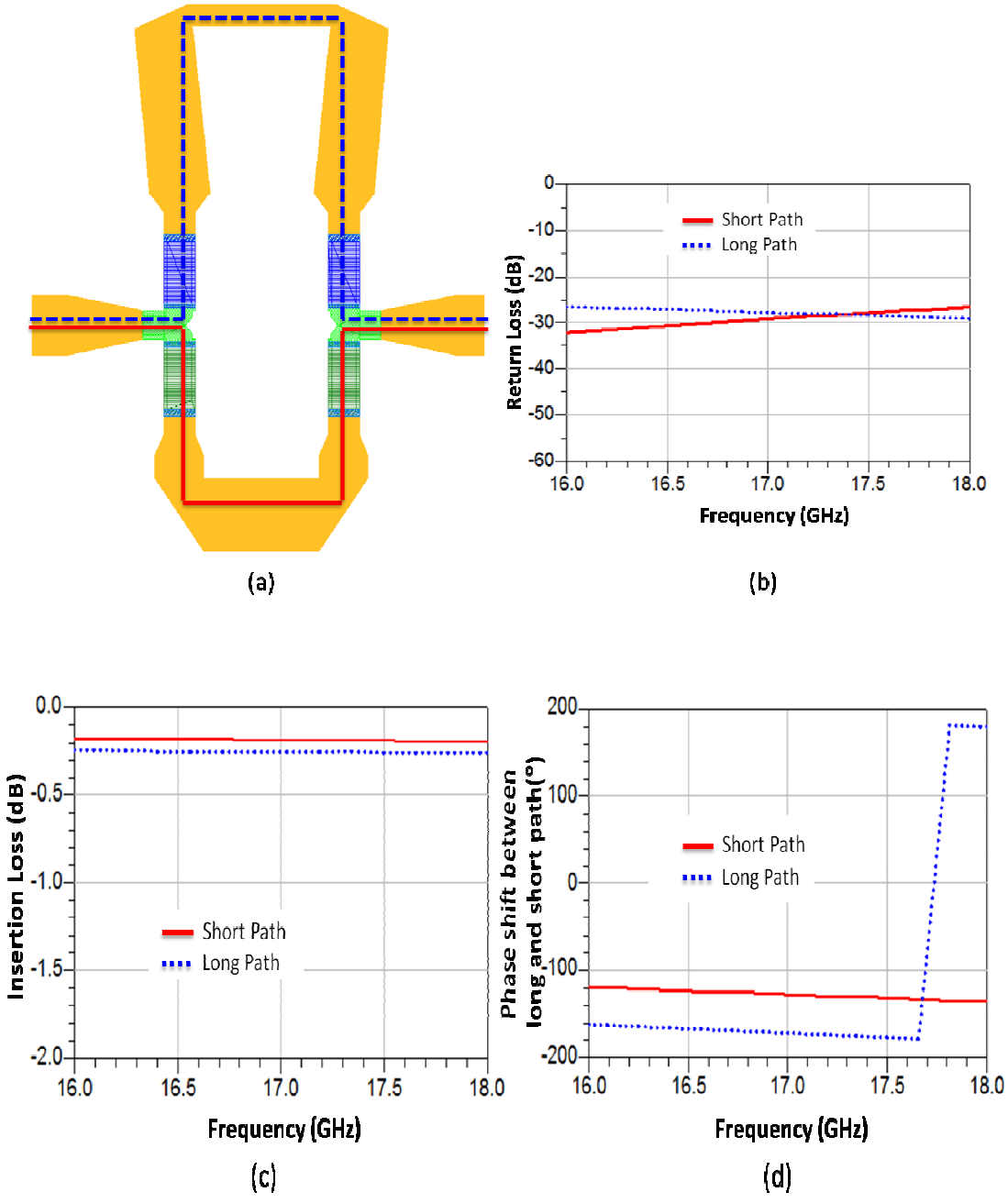


Fig.5.4: (a) Layout (b) simulated return loss (c) insertion loss and (d) phase shift of the 45^0 bit '3'.

Figure 5.5 (a-d) shows the layout and 22.5° bit simulation results for short and long path i.e. reference and delay path. The bit 4 has achieved insertion and return loss better than 0.82dB and 22dB respectively in 16-18 GHz frequency band.

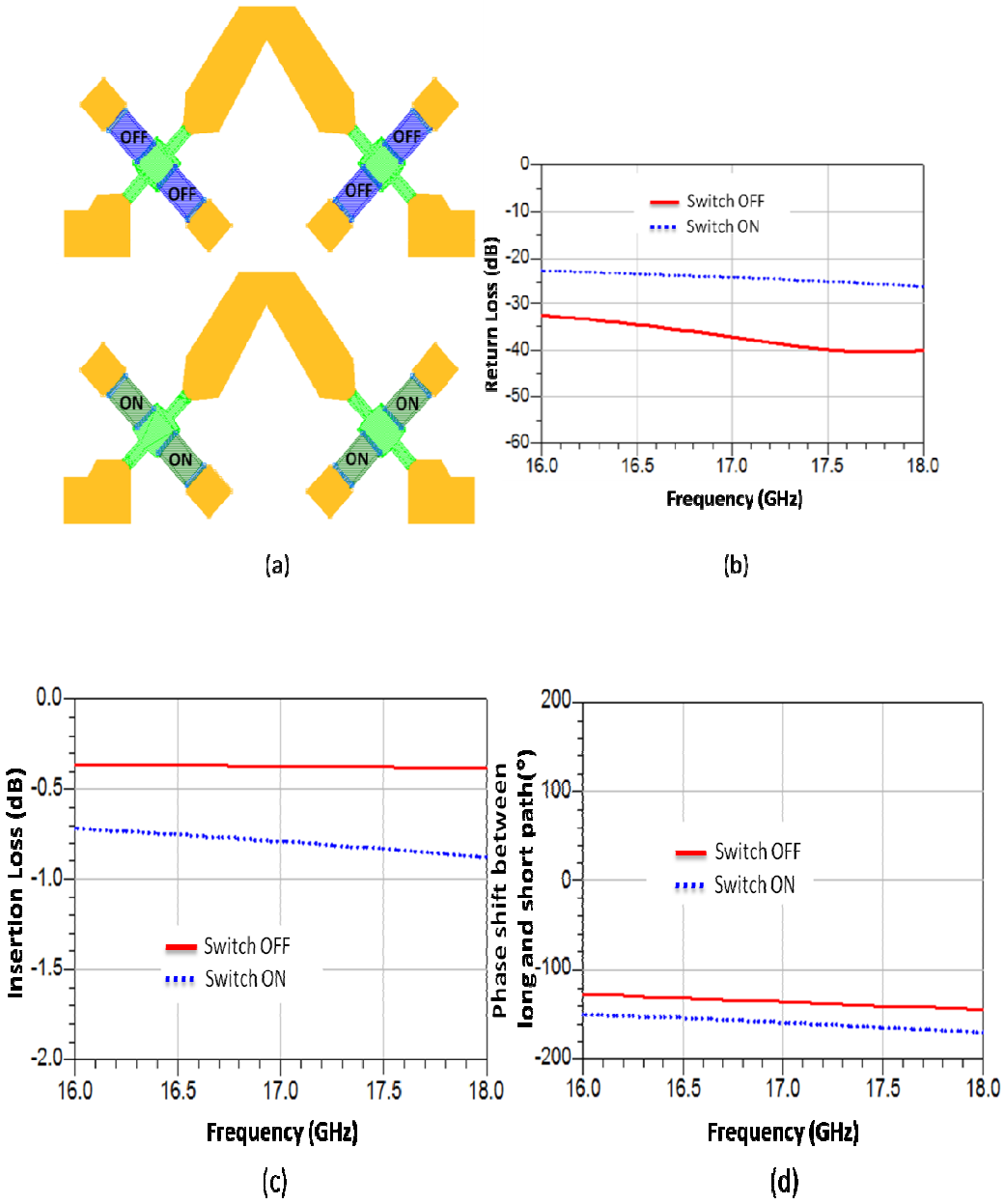


Fig.5.5: (a) Layout (b) simulated return loss (c) insertion loss and (d) phase shift of the 22.5° bit '4'.

Figure 5.6 (a-d) shows the layout and 11.25° bit simulation results for short and long path i.e. reference and delay path. The bit 5 has obtained insertion and return loss better than 0.22dB and 20dB respectively in 16-18 GHz frequency band.

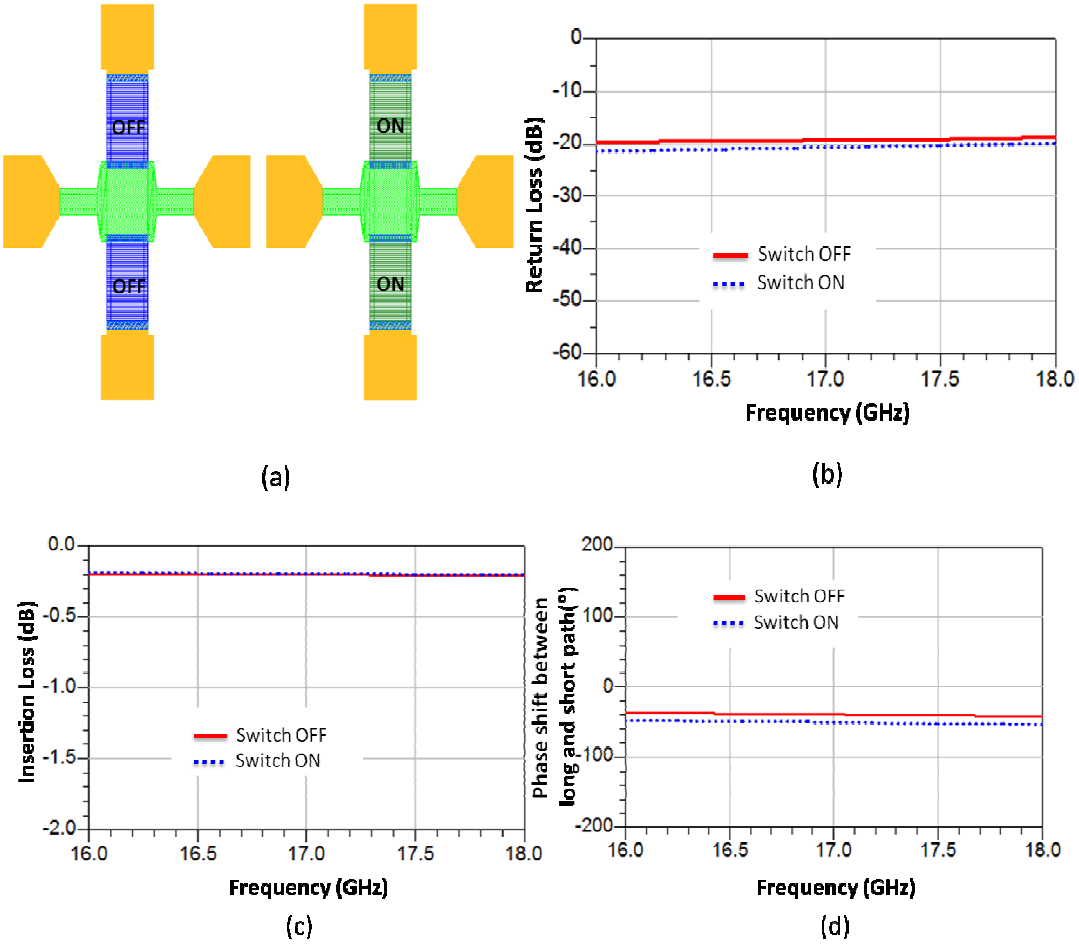


Fig.5.6: (a) Layout (b) simulated return loss (c) insertion loss and (d) phase shift of the 11.25^0 bit '5'.

The simulations show return loss better than 19 dB and insertion loss lower than 0.82dB for all bits in the 16-18 GHz frequency band. However slightly higher insertion loss is expected after fabrication since the simulation does not account for the switch contact resistance, which typically is about 0.9 Ohm. The simulated phase shift error is < 1degrees for all bits.

5.4 5-Bit Phase Shifter Simulated Performance

The performance of the integrated 5-bit MEMS phase shifters was estimated by circuitally cascading the full-wave models of the single bits using ADS momentum. Return loss better than 13dB and insertion loss better than 2.3 dB have been obtained for all 32 states in the 16-18GHz frequency band. In this case one bit higher insertion loss is expected after fabrication due to the non-zero switch contact resistance. The complete simulation results are shown in the Fig. 5.7 for the cascaded 5 bit phase shifter over 32 states.

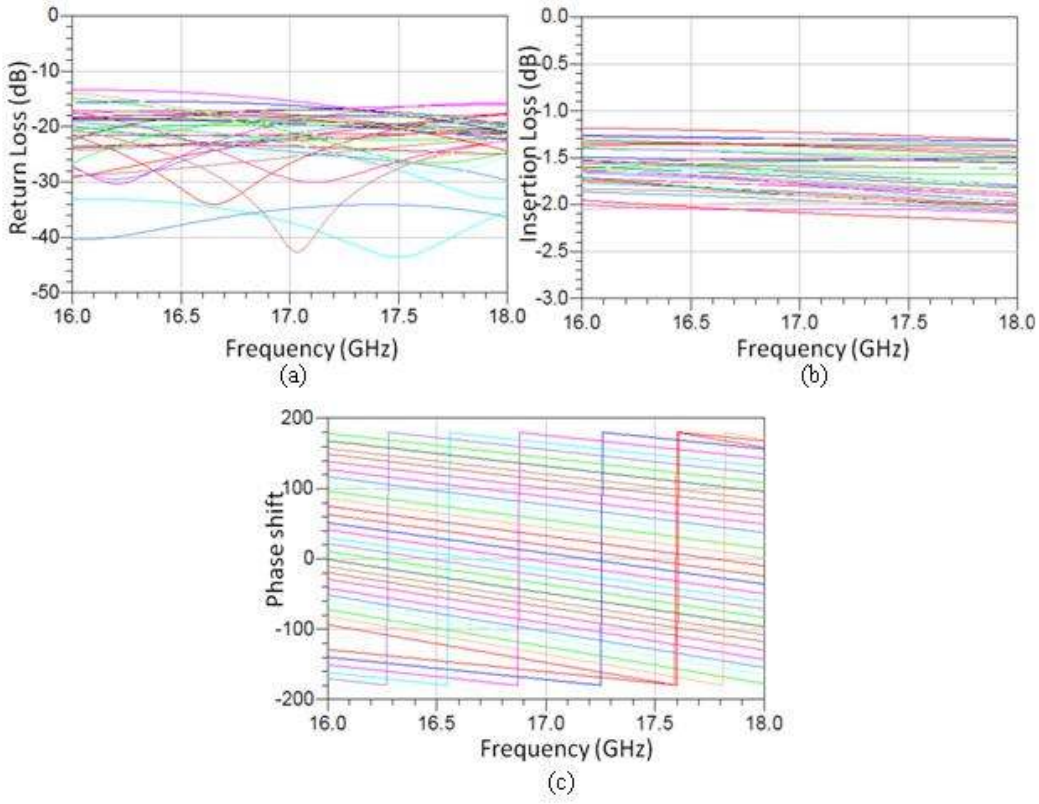


Fig. 5.7: Simulated performance for (a) return loss, (b) insertion loss and (c) phase shift of the 5-bit MEMS phase shifter for all 32 states.

5.5 Layout of 5-bit phase shifter with CPW transition

On-wafer measurements provide significant information about the functioning of the device. In view to have device test data prior to dicing of wafer and assembly of the

microstrip configuration, which is a very complex and time consuming process, via-less micro-strip to coplanar transitions have been added to this device to allow for on-wafer probe measurements by using standard GSG probes. In order to reduce the manufacturing complexity of via-less microstrip to coplanar transitions, interconnections have been designed together with a specific TRL calibration kit. This calibration kit will be used to de-embed the contribution of the CPW to micro-strip interconnection from the measurement by moving the reference plane. The first three bits have been designed using the switched line approach while remaining two bits on the loaded line approach. The layout of the microstrip phase shifter with the CPW transitions is shown in the Fig. 5.8 with the complete die size. The die size is 8.9x3.5mm.

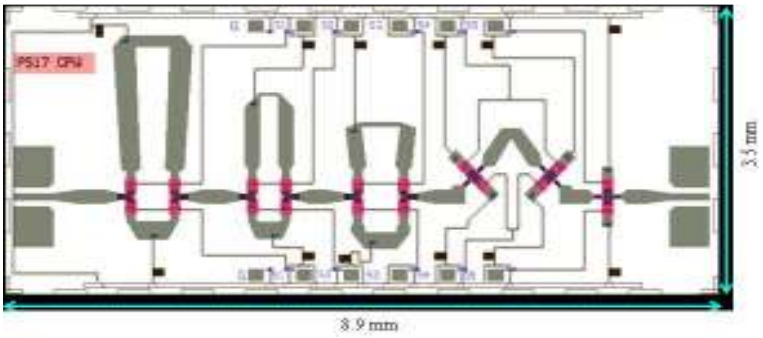


Fig. 5.8: Layout of the 5 Bit MEMS Phase shifter with CPW transition

As seen in the layout, there are six dc control pads on the top and the bottom periphery of the phase shifter. One on each marked as G are connected to ground and also shorted internally and the rest five on each side are for the control five bits. The first bit is the largest and provide 180° and subsequently followed by the 90°, 45°, 22.5° and 11.25° bits towards right. The zoomed view of the dc pads and the CPW transition are shown in the Fig. 5.9. The dimensions of DC pads and CPW RF line are as given below.

i. Pitch between DC pads is 0.6mm

ii. Dimension of DC pad is 0.2mm x 0.15 mm

iii. Dimension of CPW RF line is 0.068/0.09/0.068mm (G/S/G)

iv. The length of CPW to micro-strip transition is 0.5mm

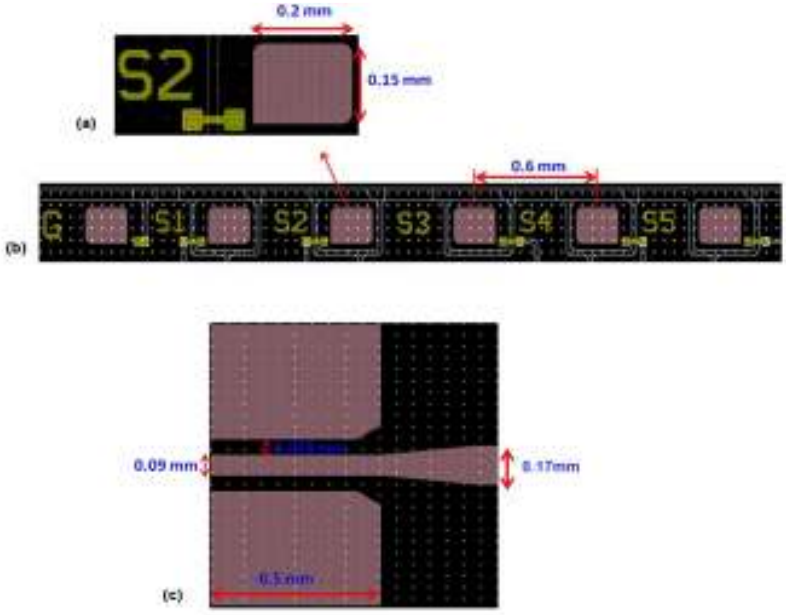


Fig. 5.9: (a) Zoomed view of a DC pad including dimensions. All DC pads have identical dimensions, (b) zoomed view of the line of DC pads in the upper part of the die. The pitch between pads is constant and equal to 0.6mm. The line in the bottom part of the die is identical to the one in the upper part. Microstrip and Coplanar versions are based on identical DC Pad dimensions, position and pitch. (c) Zoom on the CPW to Microstrip via-less interconnection.

5.6 Layout of single bits & SPST for on-wafer measurements

The single bits of phase bit i.e. 180°, 90°, 45° 22.5° and 11.25° with CPW transitions were included in the design and layout to ensure the performance at individual bit level. These measurements will provide the scope for the in depth analysis and verification of the design. This also includes the SPST switch also for testing, the basic building block of the phase shifter. The layout of the single bits and switch are shown in the Fig. 5.10. This layout becomes part of the wafer level layout. Two sets of this layout have been included in the wafer level layout. The TRL kit developed will be used to characterize the RF parameters of these structures.

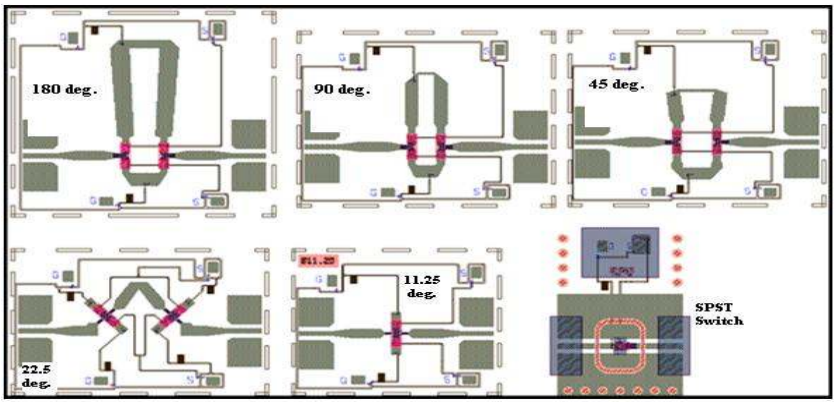


Fig. 5.10: Layout of single bits of including CPW transition and Ohmic series switch for on-wafer measurement.

5.7 On-wafer TRL Calibration Kit

The layout of the 17GHz TRL calibration kit is depicted in Fig. 5.11. The calibration kit will allow on-wafer measurements of the phase shifter single bits as well as of the 5-bit device with CPW transition in the defined frequency band. Since the coplanar to microstrip interconnection are via-less, it was envisaged to use such a calibration kit to perform on-wafer TRL calibration so as to move the measurement reference plane. In this way the measurements will not include the loss of the via less interconnection and provide the accurate measurements.

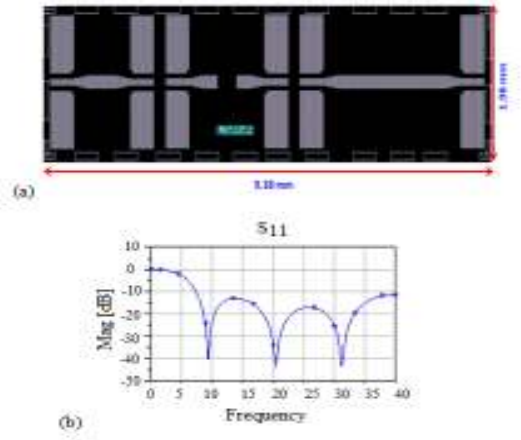


Fig. 5.11: (a) TRL calibration kit layout and (b) LINE simulated return loss.

5. 8 Layout of the Microstrip Configuration

The layout of the microstrip version is shown in the Fig. 5.12. The microstrip version has the same design concept as of the CPW configuration except the transition part. The pitch and size of the dc bias pads is exactly same as explained in section 5.5 for the CPW version. The inner line shows the future scope for the zero level packaging.

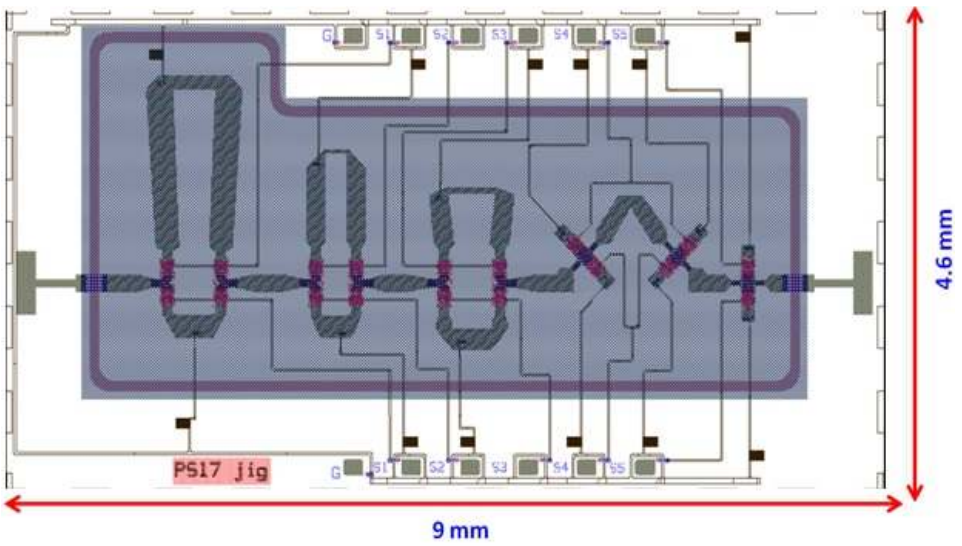


Fig. 5.12: Layout of the 5-bit microstrip MEMS phase shifter.

5.9 Wafer Level Layout Plan

5.9.1. Types of devices

Table 5.1 shows the summary of the number of various types of devices incorporated into the complete wafer layout. This consists of various types of configurations namely microstrip, microstrip with CPW transition, phase shifter with LC section for jig level testing, single bit cells with CPW transitions and TRL calibration kit. The numbers vary according to the requirement for their usage. The number of the microstrip configuration was incorporated in large numbers as these are required to be used in the system. The above die layout shows the area of the die to be encapsulated with wafer level packaging.

Table 5.1: Shows the type and number of all of devices incorporated in the wafer layout

Sl. No.	Devices	Name Pattered on the Die	Width (mm)	Height (mm)	Replicas per Wafer (Nos.)
D1	Phase Shifter µstrip	PS17µS	9	4.6	62
D2	Phase Shifter (CPW Configuration)	PS17CPW	8.9	3.5	20
D3	Phase Shifter + LC matching section	PS 17 jig	9	4.6	10
D4	Single bit cells for on-wafer measurements	Bit 180°/90°/45°/ 22.5°/11.25°	--	--	2
D5	TRL Cal Kit	PS_17_Kit_C	9.3	1.9	4

5.9.2 Layout of devices on 4'' mask

The complete wafer layout displaying all type of devices is shown in the Fig.5.13. This layout also consists of the foundry structures to verify the fabrication process.

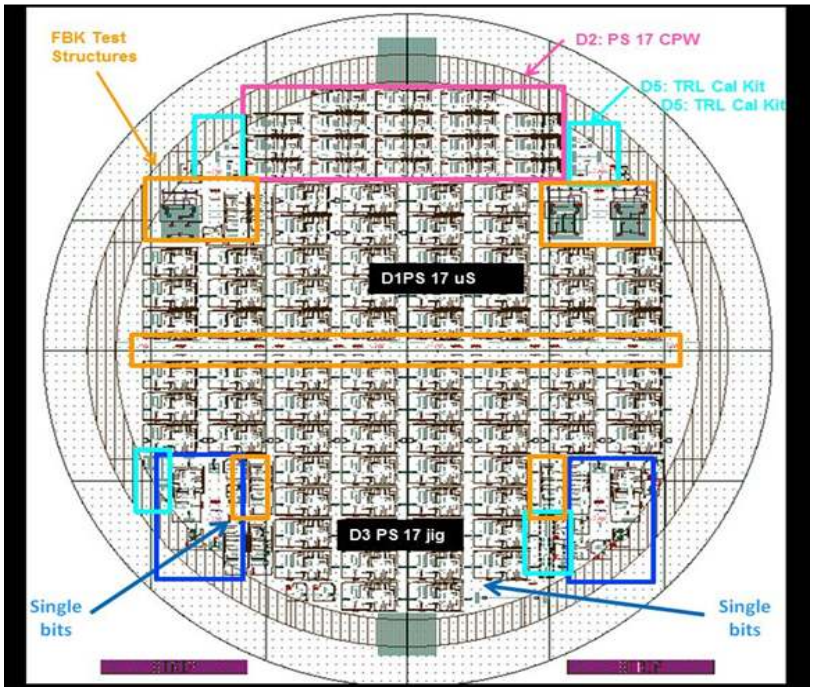


Fig.5.13: Complete 4" mask layout of the phase shifter.

5.10 Analysis of MEMS structures

Cantilever RF switches are very performing in terms of isolation and return loss but particular attention needs to be devoted to the ohmic contact in order to obtain repeatable, stable and very low contact resistance. The switch impacts the phase shifter performance to a great extent.

5.10.1 Equivalent Circuit

The Fig. 5.14 shows the layout and simplified equivalent circuit of the MEMS Cantilever Series Ohmic Switch. It was analyzed that the designed switch has R_{on} and C_{off} are of the order of 0.9 ohm and 10 fF in the 0-30 GHz frequency range.

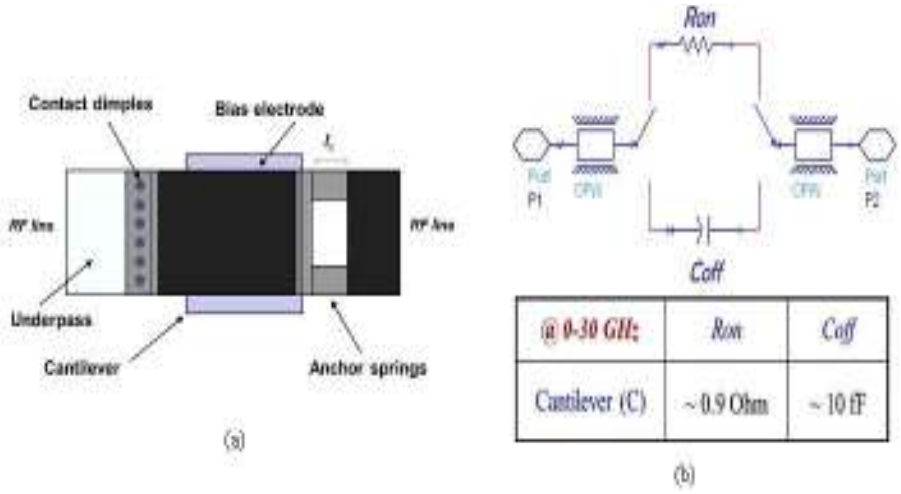


Fig. 5.14 (a) Layout and (b) simplified equivalent circuit of the Series Ohmic cantilever MEMS Switch.

5.10.2 Electromechanical Analysis

Analysis has been done to optimize the most critical aspects of the electromechanical design. The following parameters were studied in detail in order to ascertain the stable operation.

i. Actuation voltage

ii. Contact force due to series resistance

iii. Deformation arising because of stress gradient

ANSYS Multiphysics simulations have been used to trade-off between contact force, restoring force and actuation voltage. Switches with different spring lengths *ls* have been analyzed including the case of *ls* = 0 µm. Figure 5.15 shows the simulated pull-in voltage, contact force and contact pressure on the six contact bumps. The simulation shows that a spring length *ls*=10µm can improve the contact force per bumps with respect to the case *ls* = 0 µm.

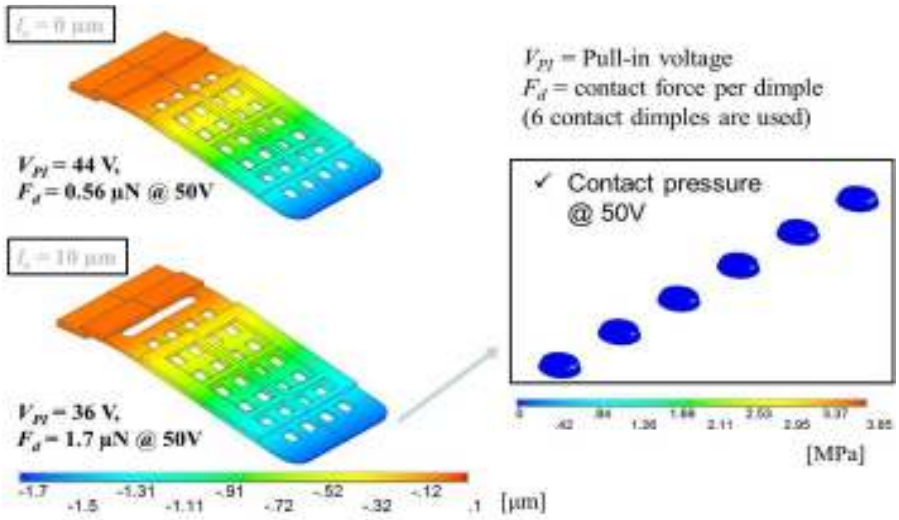


Fig. 5.15: (a) Layout and (b) simplified equivalent circuit of the Series Ohmic cantilever MEMS Switch.

The stress gradient is quite significant for long term operation; this has been analyzed and taken into account as it may cause an upward bending of the cantilever. This aspect consequently varies with actuation voltage and contact force. Figure 5.16 and 5.17 shows the tip bending versus the stress gradient and the cantilever stiffness as a function of the stress gradient for different spring lengths *ls*. It has been analyzed that even a small spring is very useful to reduce the cantilever sensitivity to stress gradient providing a more robust and repeatable design. As shown in the figure there is significant variation in the tip bending stress between zero spring length and with 10µm spring length. It has also been observed that this variation is negligible due to further variation in dimensions of spring length.

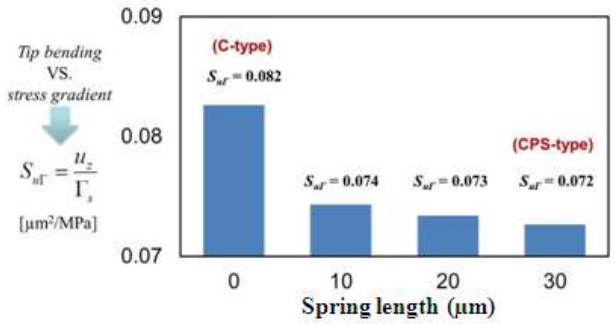


Fig. 5.16: Tip bending versus the stress gradient for different spring lengths ls.

Similarly stiffness analysis shows that a small spring length *ls* = 10 μm has significant reduction in stress gradient with respect to zero spring length. It also shows that further increase in spring length does not help in stiffness reduction.

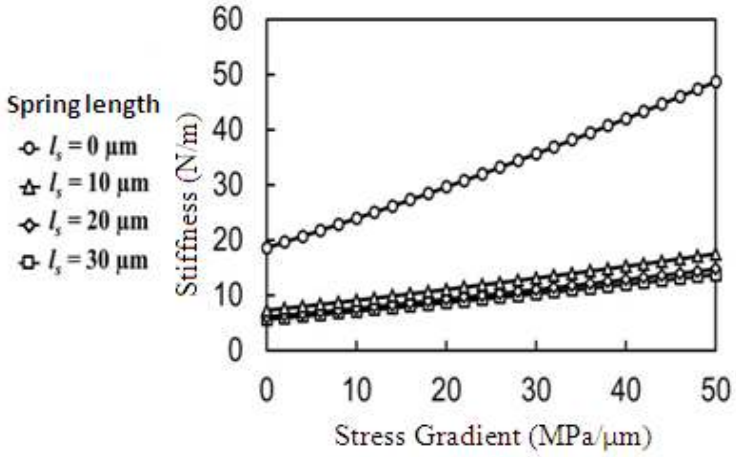


Fig. 5.17: Cantilever stiffness as a function of the stress gradient for different spring lengths *ls* = 10, 20, 30 and 40 μm.

The contact area over the dimples is another important parameter that has been analyzed. For high stress gradient, the contact area may be larger and also the electrostatic force is higher (lower residual gap after the pull-in). Therefore the position of the contact dimples has been optimized. Figure 5.18 (a-c) shows the parametric analysis of the contact force for different bump spacing Δd and distance from the cantilever tip Δc in the cases of 0 and 15Mpa/μm stress gradient.

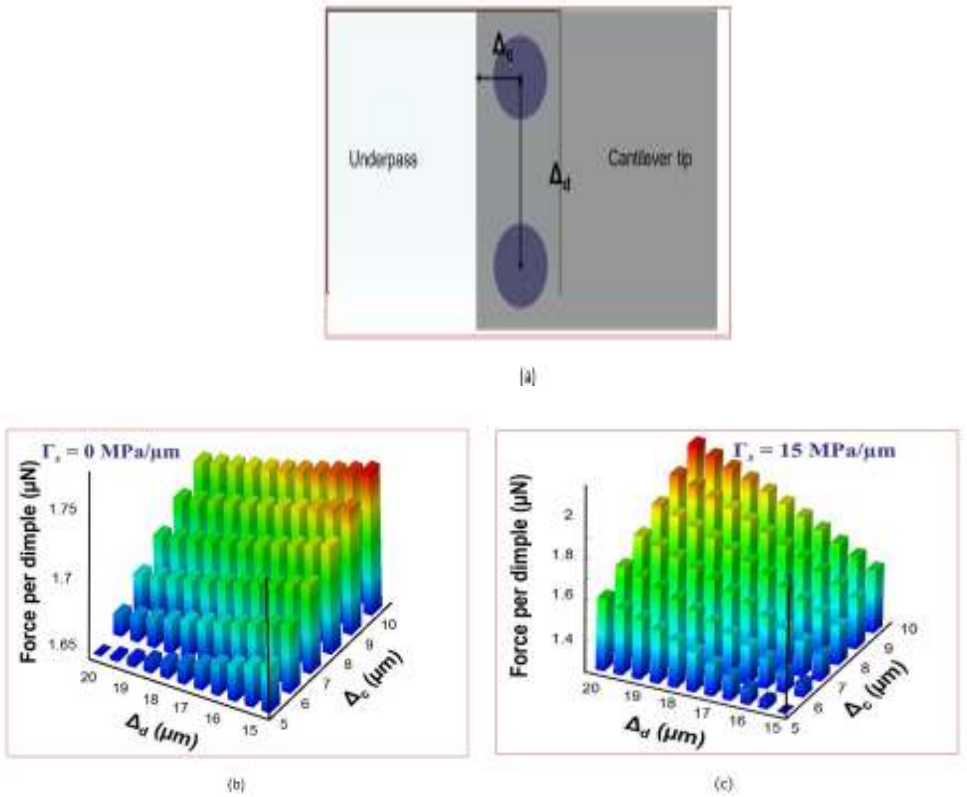


Fig. 5.18: (a) Layout and definitions (b) analysis in case of zero stress gradients and (c) analysis in case of 15MPa/µm stress gradient.

Analysis concludes, the force on dimple (computed @ 50V increases) if the dimples are closer to each other and more distant from the cantilever tip, in case of zero stress gradients. On the other hand, for stress gradient higher than 15 MPa/µm the contact force increases and it is better to have contact dimples more distant to each other. As a trade-off between high contact force and low sensitivity to stress gradient it was optimized *ls*=10 µm Δd = 18 µm and Δc = 10 µm as the best switch parameters.

Summary

The design and simulation of the single bits and integrated 5-bit CPW with microstrip version has been carried out. The results have shown a consonance with the design targets. However one bit higher insertion loss is expected due to the zero contact resistance assumption during

the simulation. Electromechanical simulations have been done with more emphasis on the stable operation of the MEMS part. The critical parameters such as tip bend force have been analyzed uniquely.

5.11 Design of 5-bit Switched Line Topology on GaAs

The design and simulation of 5-bit phase shifter based on switched line topology using GaAs has been performed keeping in view of the objectives like low actuation voltage and fabrication in India using GaAs process foundry. More over GaAs material is highly suitable for the high frequency applications due to its natural semi insulating property.

To realize a 5-bit phase shifter, individual bits were designed and simulated before the design of the integrated phase shifter. This methodology was adopted to ensure the higher phase accuracy. The individual five phase shifter bits consist of a common reference line length and have a relative phase difference path of 11.25°, 22.5°, 45°, 90° and 180°. There are thirty two possible states with step of 11.25°. Each bit requires two sets consisting of two switches which control the signal in the path for transmission or reflection. This design was carried out with shunt capacitive switches hence switches were placed at $\lambda/4$ distance from the junction. The length of switched line phase shifter for every reference (L) and delay paths (L+ΔL) for each phase bit was calculated with reference to the phase change requirement as per equation (1).

$$\Delta\Phi = \Phi_2 - \Phi_1 \quad (1)$$

Where

Φ_2 - Phase of delay path

Φ_1 - Phase of reference path

$\Delta\Phi$ - Differential phase shift

The individual bit layout is shown in the Fig. 5.19. It may be noted that the delay path is increasing from the 11.25° to 180° bit to meet the phase delay requirements.

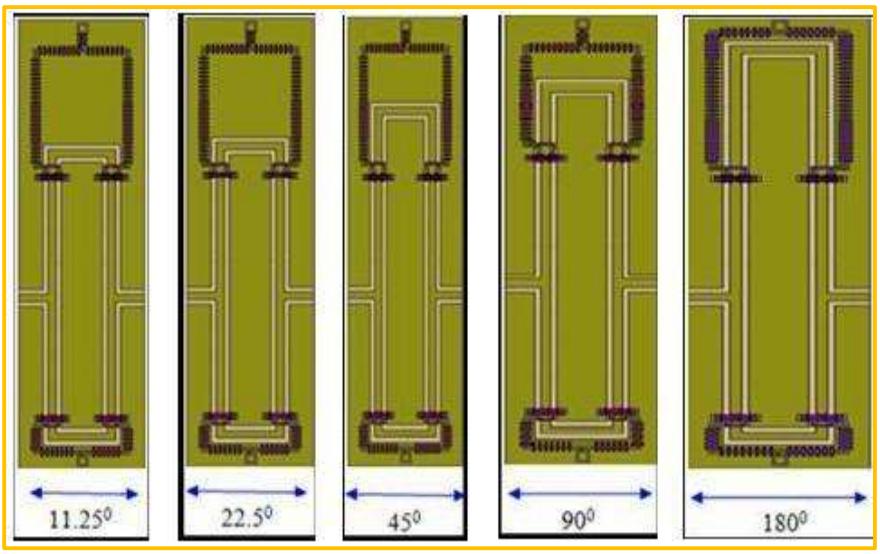


Fig. 5.19: Individual 5-bit layout for fabrication.

The Electromagnetic simulation for the individual bits has been carried out using the 3D High frequency Structure Simulation software (HFSS). It provides the full wave electrical simulation. However the basic design was carried out using MWO design package. The RF simulation was performed keeping the reference path switches in the up state for the reference path and putting down for the delay path alternatively. This process was repeated for the five bits respectively. Optimization was carried out for every bit to achieve the precise phase accuracy in the simulation. The insertion loss increased with the cascade of bits in comparison to the individual bits. The electrostatic and the mechanical simulation for the pull in & contact voltage including the mechanical resonant frequency were also carried out using the Coventorware software.

5.12 Integrated Phase Shifter Simulation Results

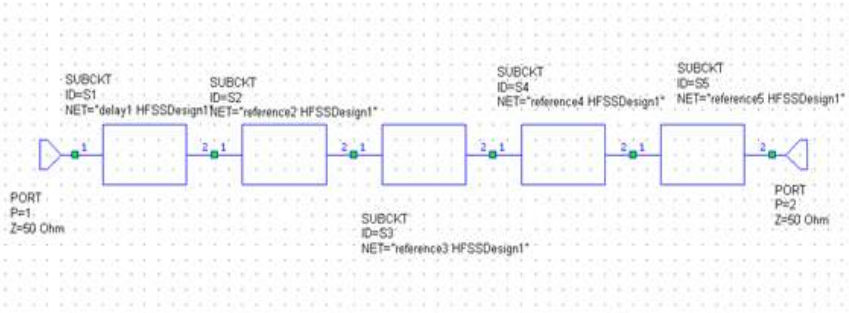
The integrated 5-bit Phase Shifter model is quite large in size and requires long simulation time. To avoid long process time in 3D EM simulators, the individual bit results

have been taken from HFSS and these were exported to AWR MWO to carry out the RF simulations for the integrated five bits.

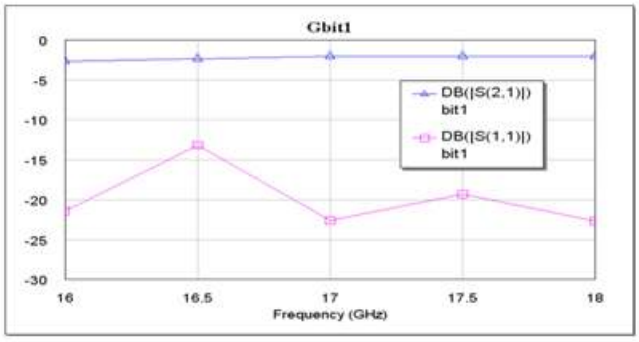
5.12.1 Simulation Results of Principal Bits

The results of the principal bits are shown in this section. The performance of the 11.25° bit is shown in Fig. 5.20. The other four bits namely 22.5°, 45°, 90° and 180° were put in the reference path while only 11.25° phase bit was operated in the delay path. The 11.25° bit has shown insertion and return loss as 2.1 dB and 22 dB respectively at 17 GHz.

5.12.1.1. 11.25° phase bit



(a)

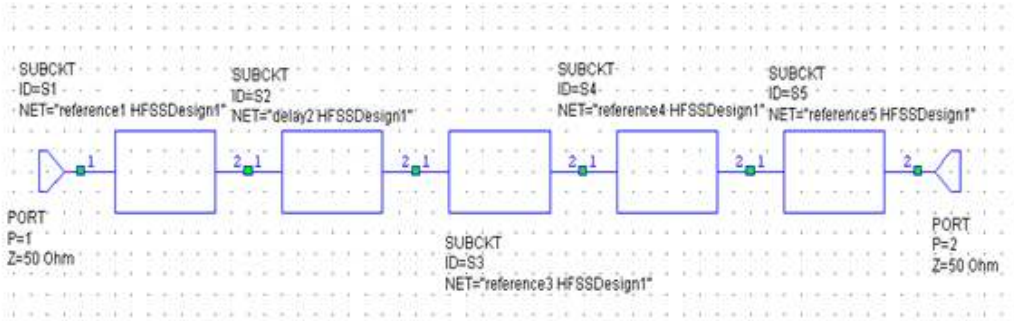


(b)

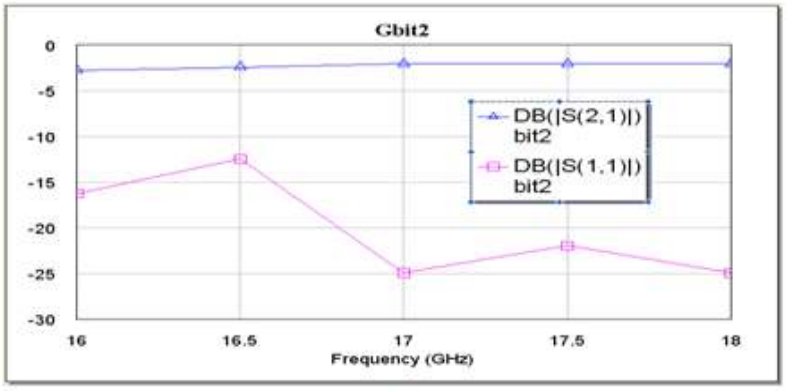
Fig. 5.20: (a) MWO image and (b) Insertion and Return loss for 11.25° bit1.

5.12.1.2 22.5° phase bit

The performance of the 22.5° bit is shown in Fig. 5.21. The other four bits namely 11.25°, 45°, 90° and 180° were put in the reference path while only 22.5° phase bit was operated in the delay path. The 22.5° bit has shown insertion and return loss as 2.0dB and 25dB respectively at 17GHz.



(a)



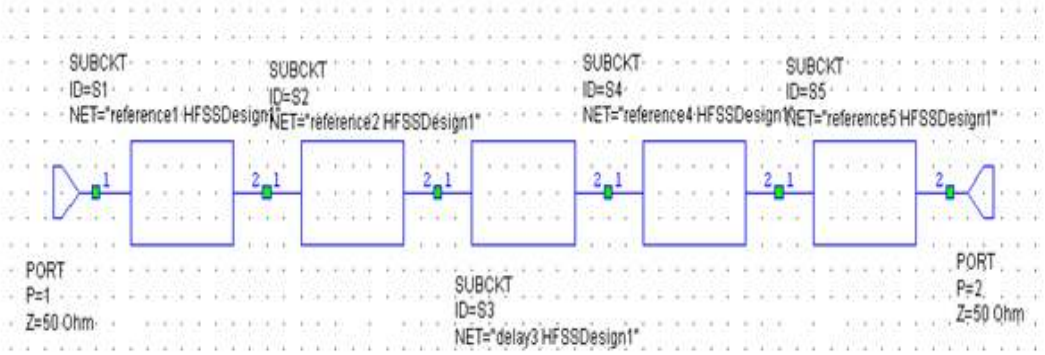
(b)

Fig. 5.21: (a) MWO image and (b) Insertion and Return loss for 22.5° bit2.

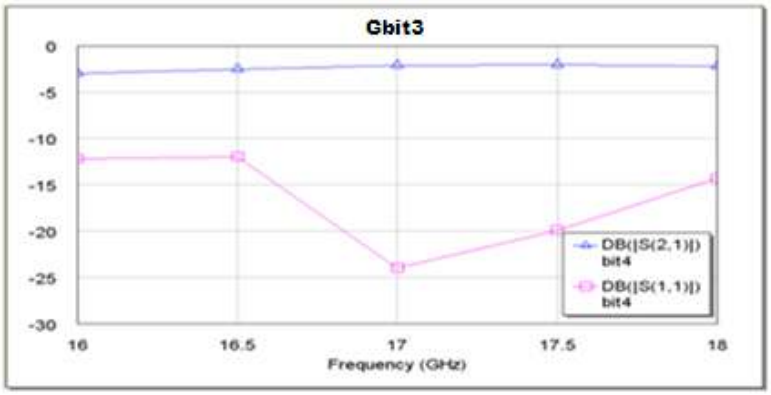
5.12.1.3 45° phase bit

The performance of the 45° bit is shown in Figure 5.22. The other four bits namely 11.25°, 22.5°, 90° and 180° were put in the reference path while only 45° phase bit was

operated in the delay. The 45° bit has shown insertion and return loss as 1.8dB and 24dB respectively at 17GHz during integrated simulation.



(a)

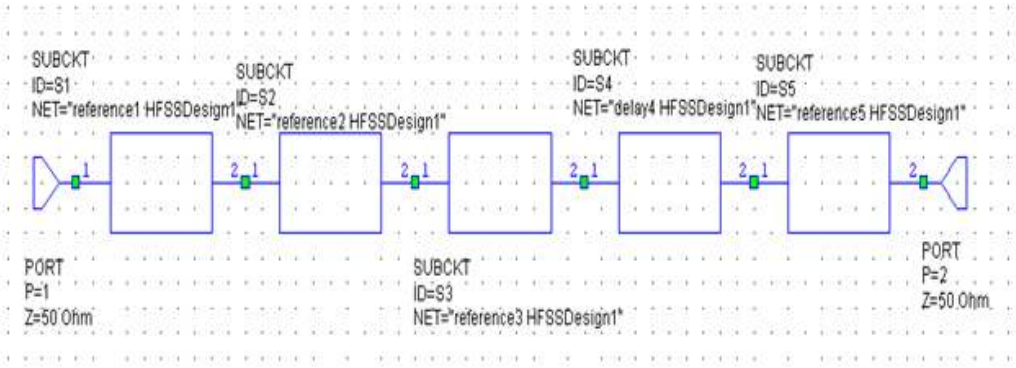


(b)

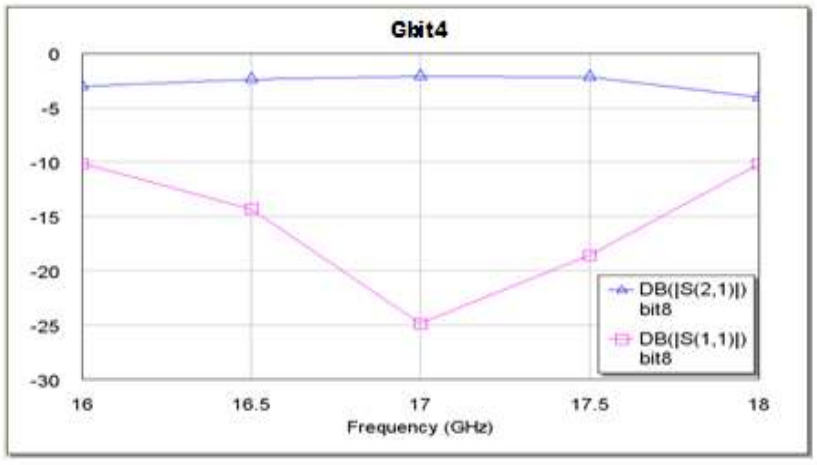
Fig.5.22: (a) MWO image and (b) Insertion and Return loss for 45° bit3.

5.12.1.4 90° phase bit

The performance of the 90° bit is shown in Fig. 5.23. The other four bits namely 11.25°, 22.5°, 45° and 180° were put in the reference path while only 90° phase bit was operated in the delay. The 90° bit has shown insertion and return loss as 1.8dB and 25dB respectively at 17GHz.



(a)

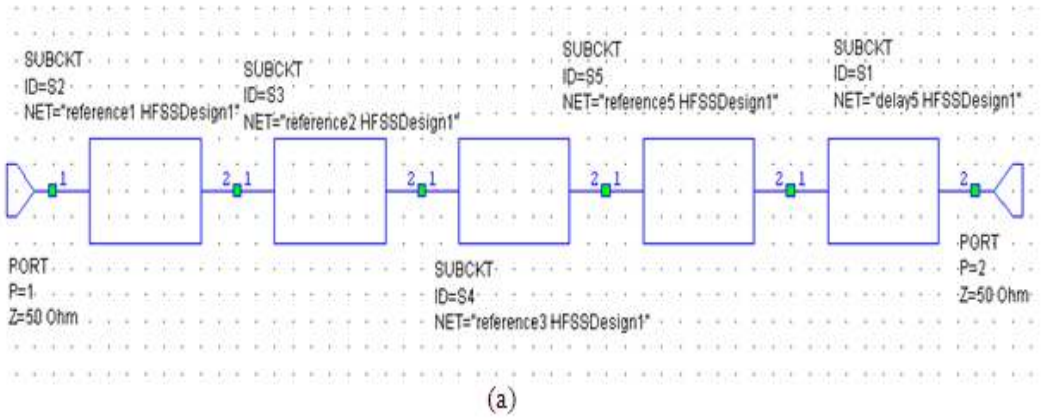


(b)

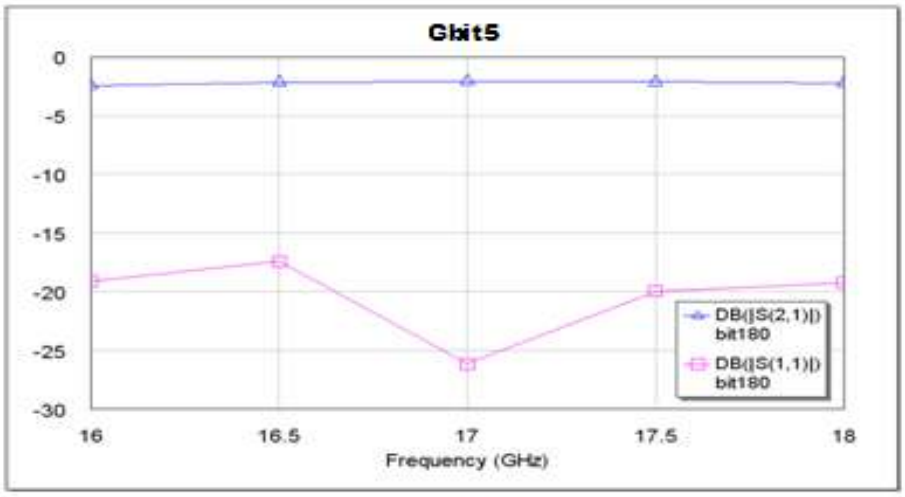
Fig.5.23: (a) MWO image and (b) Insertion and Return loss for 90° bit4.

5.12.1.5 180° phase bit

The performance of the 180° bit is shown in Fig. 5.24. The other four bits namely 11.25°, 22.5°, 45° and 90° were put in the reference path while only 180° phase bit was operated in the delay. The 180° bit has shown insertion and return loss as 1.8dB and 26dB respectively at 17GHz.



(a)



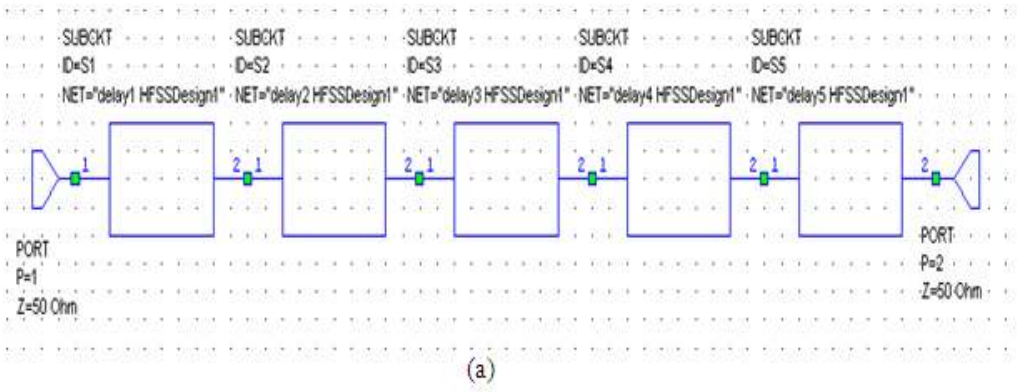
(b)

Fig.5.24: (a) MWO image and (b) Insertion and Return loss for 180° bit5.

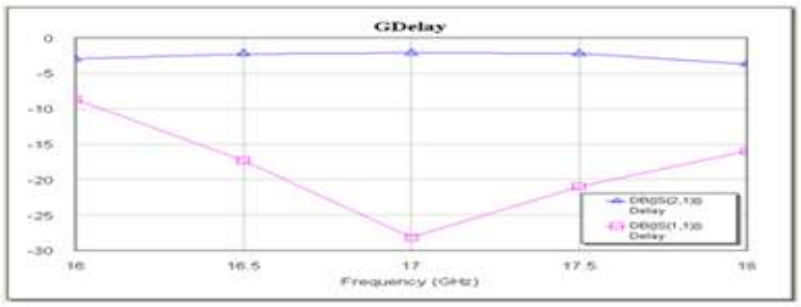
5.12.2 Simulation Results of 5-bit Phase Shifter

5.12.2.1 Integrated 5-bit delay path result

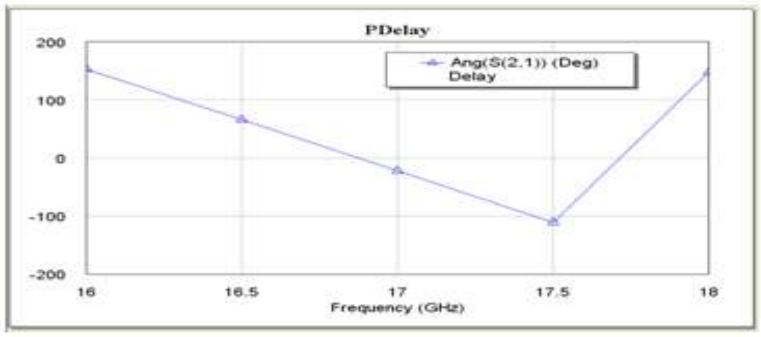
All the five bits namely 11.25°, 22.5°, 45°, 90° and 180° were put in the delay path to simulate the S parameters. The performance of the integrated 5-bit delay path is shown in Figure 5.25 (a-c). The 5-bit delay path has shown insertion and return loss as 1.8dB and 26dB respectively at 17GHz.



(a)



(b)



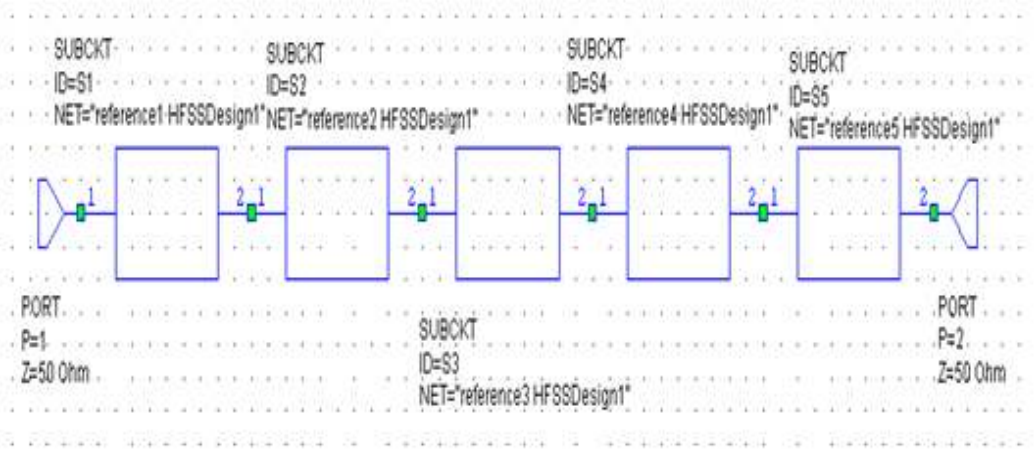
(c)

Fig.5.25: (a) MWO image, (b) Insertion and Return loss and (c) Phase for 5-bit delay path.

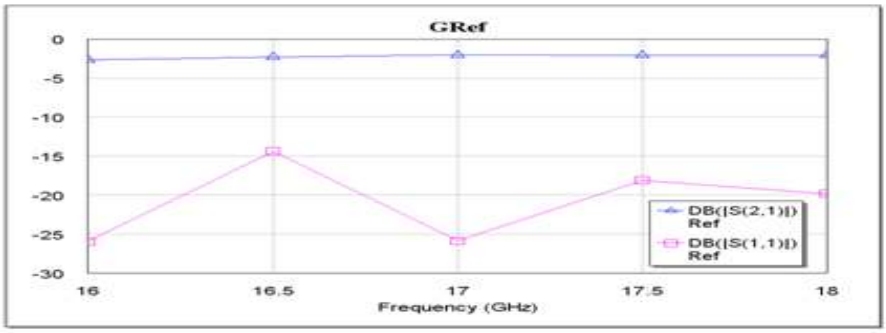
5.12.2.2 Integrated 5-bit reference path result

All the five bits namely 11.25°, 22.5°, 45°, 90° and 180° were put in the delay path to simulate the S parameters. The performance of the integrated 5- bit delay path is shown in

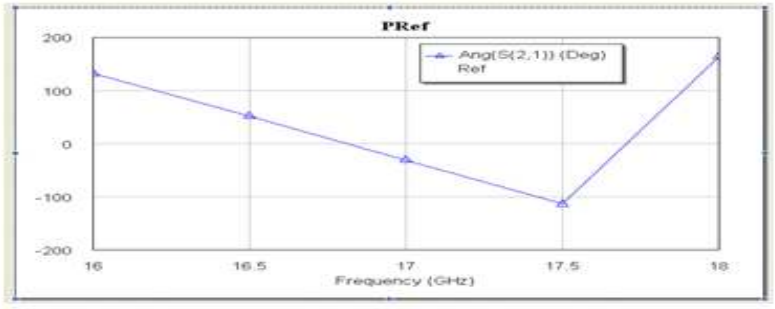
Figure 5.26 (a-c). The 5-bit reference path has shown insertion and return loss as 1.8dB and 25dB respectively at 17GHz.



(a)



(b)



(c)

Fig. 5.26: (a) MWO image and (b) Insertion and Return loss and (c) Phase for 5-bit reference path.

The integrated layout is shown in the Fig. 5.27. All the 5-bits have been cascaded in the configuration. The die size is 9.7x7.3mm.

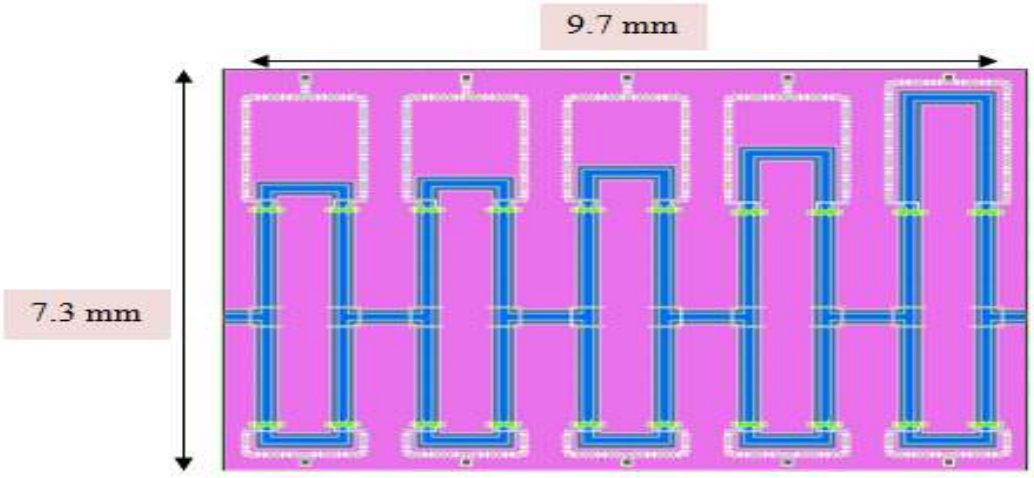
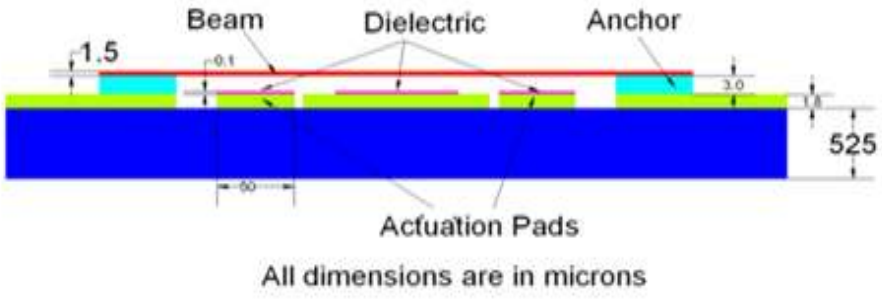


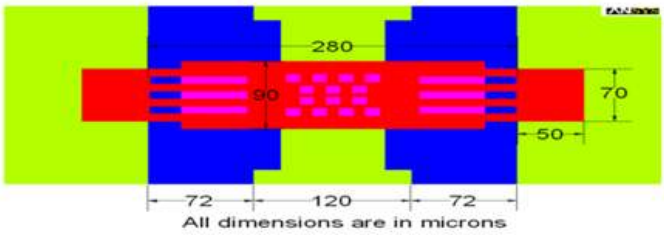
Fig.5.27: Integrated layout of the 5-bit Phase Shifter on GaAs.

5.13 Electromechanical Simulation

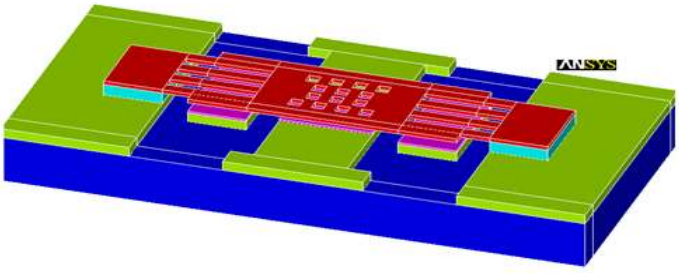
The electromechanical simulations were performed using Coventorware and ANSYS. The cross section, top and 3D views are shown in the Fig. 5.28 (a-c) displaying the dimensional details of different details.



(a)



(b)



(c)

Fig.5.28: (a) Cross sectional view, (b) top view and (c) 3D view of the switch part.

The pull-in, contact and hysteresis analysis was carried out using Coventorware and the results are displayed in the Fig. 5.29. A nearly linear deflection has been obtained for a travel of 1.6µm at a voltage of 31.8V up to the pull in point. Beyond the pull in voltage point a sudden snap down was observed. The membranes were analyzed for the hysteresis response which is quite crucial for the smooth operation of the switch. The contact point was observed at 35.2V having air gap as 2.9µm and the pull back phenomenon also called restoration force, occurred at the 22V after removal of the actuation potential. The pull back shows that the design has the sufficient restoration force required for the stable operation of the device. The simulations were carried out using FEM model of the switch. The mechanical resonance is significant from the structural integrity point of view. The membrane was subjected to modal analysis to estimate the resonant frequency so as to analyze the effect of vibrations when

implemented in field applications. The results are shown in the Table 5.2 for the six modes. The structural resonance of the first mode was obtained as 23.208 KHz through the modal analysis.

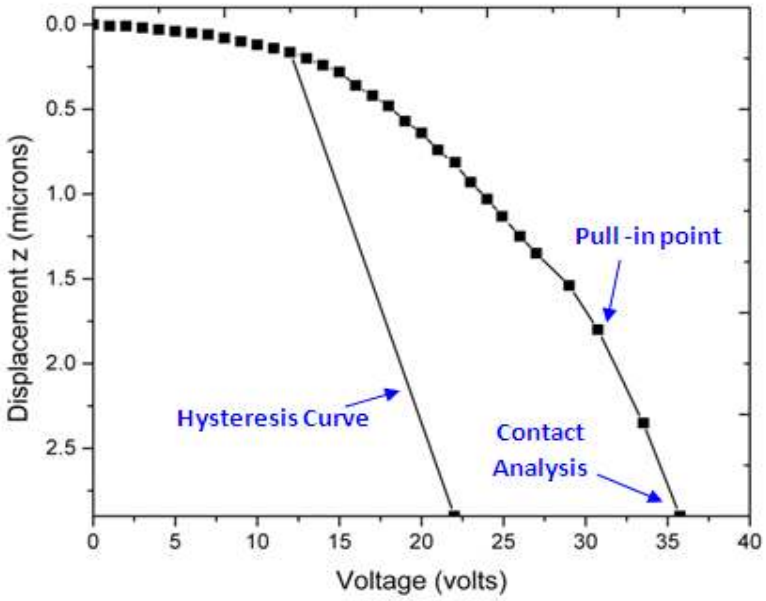


Fig. 5.29: Pull-in point, Contact and Hysteresis Analysis curve.

Table 5.2: Modal Analysis for Resonance Frequency

Mode No.	**Modal frequency (KHz)**
1	23.208
2	63.368
3	72.149
4	126.493
5	130.607
6	218.561

Summary of Simulation Results

The summary of design and simulation of the 5-bit phase shifter on GaAs has been presented in the Table 5.3.

Table 5.3: Summary of 5-bit Phase Shifter on GaAs

Substrate Type/ Thickness	GaAs 525 μm				
CPW (Width/Gap) Impedance	120μm/72μm 50 Ω				
Reference Length	5400 μm				
Delay Length	11.25°	22.5°	45°	90°	180°
Feed Line length (Input-Output)	500 μm				
Phase error	± 2^0 each state				
Beam Dimensions Pull in Voltage	Length-264μm, width- 90 μm, thickness- 1.5 μm 31.8V				
Actuation Area	90 x 50 μm^2 (2)				
Size	9.7 mm x 7.3 mm				

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CHAPTER 6

Fabrication and Process Inspection

Surface micromachining is the established technique for the RF MEMS devices. The building of layers of materials on the substrate requires set of masks for depositing the different layers as per the specific design. This process is not constrained by the type of the substrate. There is a wide choice of thin film materials to be used for the complex geometries. Surface micro machined devices typically uses three types of components namely sacrificial component also called spacer layer, micro structural component and the insulator component. Polycrystalline silicon is common material used as the layer material. There are basically three critical aspects of mechanical nature that result from the surface micromachining. There are adhesion of layers, interfacial stresses, stiction and should be taken care during fabrication in order to meet the design requirements.

6.1 Process Description

The basic elements that are required to be fabricated are the series type of electrostatic actuated MEM switches having mobile metallic bridges. These are cantilever beams processed together with high resistive polysilicon actuation pads and high value resistors and DC blocking capacitors. The fabrication process (FBK) is optimized for the fabrication of RF MEMS switches on a high resistivity silicon substrate. The process is also capable to provide suspended inductors, blocking capacitors and DC blocking resistors together with basic RF passive components like co-planar wave guides, T junctions, bends and fixed air bridges.

The devices are fabricated on p-type, 200μm thick double polished, >5 kΩ-cm high resistivity silicon FZ 4" wafers. The first step of fabrication process has been the realization of an insulating layer of 1μm thick of silicon oxide. The layer was grown by wet thermal oxidation at 975°C. The charges trapped at the silicon oxide interface can induce a conductive channel that increases the losses on the substrate by capacitive coupling. To reduce this effect an annealing at 975°C for 50 minutes in nitrogen atmosphere has been performed. A 630nm thick layer of polysilicon is then deposited by low pressure chemical vapour deposition (LPCVD) at 630°C as shown in Fig. 6.1(a). The polysilicon layer is then ion implanted using boron ions (BF2) at 120KeV. The dose can be adapted depending on the required resistivity. Typically $6.2x10^{14}$ B/cm^2 was used to obtain a sheet resistance of about 1600 Ohm/□. With the first lithography step the polysilicon biasing line and actuation electrodes are defined and then dry etched. To improve the contact resistance small dimples ($4x4\mu m^2$) of polysilicon are realized to define exactly the number and position of contact points between the movable membrane and the underpass signal line. After removing the photoresist layer, the implanted B ions are diffused and electrically activated by an annealing at 925°C for 1 hour in nitrogen atmosphere to obtain the required doping profile. A 300nm thick insulating layer of SiO_2 is deposited by low pressure chemical vapour deposition. A flexible fabrication process for RF MEMS device using TEOS (Tetraethyl orthosilicate) was carried out.

A conductive metal layer (Al 1%Si) is then deposited by sputtering. A diffusion barrier (Ti/TiN) is used to avoid spiking at the polysilicon interface and hillocks formation on the top. The resulting multilayer is composed of 30nm Ti, 50 nm TiN, 410 nm Al 1%Si, 60 nm Ti and 80 nm TiN. The thickness of the multi-metal underpass and the polysilicon actuation electrodes has been the same in order to avoid distortions in the actuated bridge The metal is defined by the third lithography and dry etched as shown in Fig.6.1 (b).

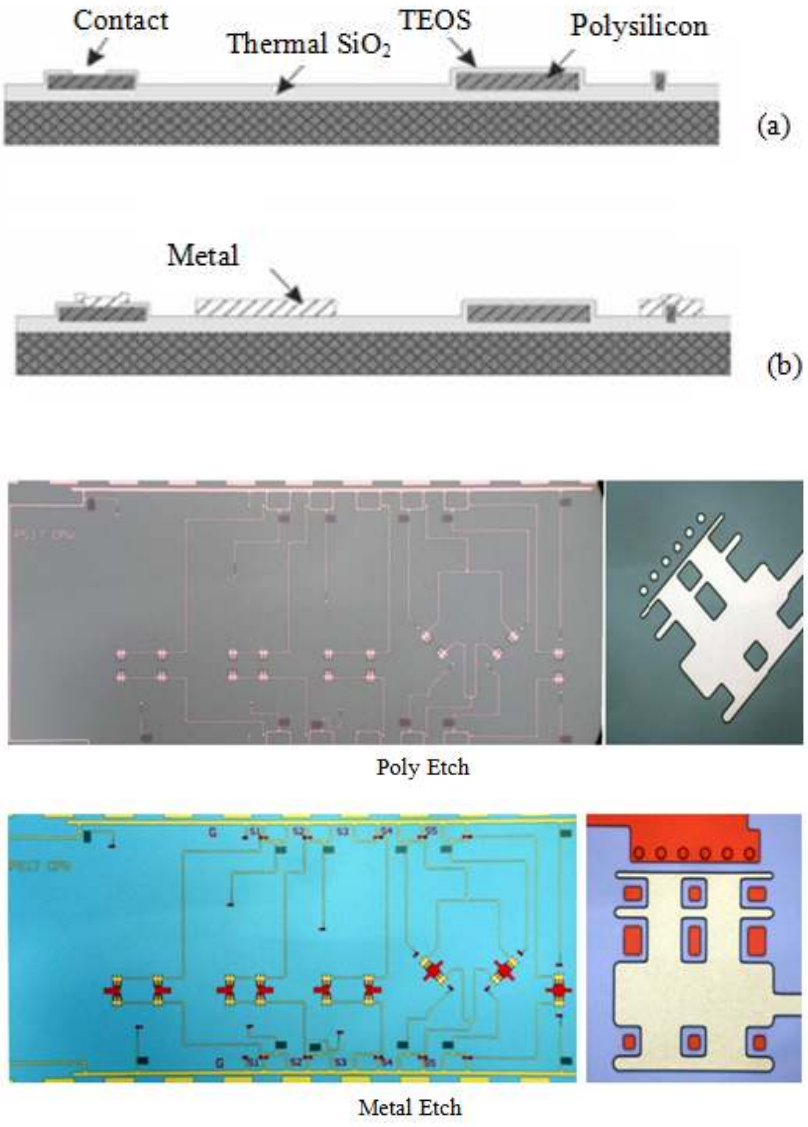


Fig. 6.1: (a) thermal oxidation; poly-silicon, TEOS deposition and contact opening and (b) metal deposition and patterning. The images display the view after poly and the metal etch.

A 100nm thick SiO_2 dielectric layer by low temperature oxide (LTO) is deposited by LPCVD at 430°C using Silane. The fourth lithography step defines the vias in the LTO that are dry etched in the TEGAL 903 as shown in the Fig. 6.1(c). A 5nm Cr 150 nm Au layer is deposited by electron beam gun to be used both as electrically floating metal layer over capacitors and to reduce the metal-Au resistance inside vias. The Cr is used as adhesion layer

because gold has a very poor adhesion over silicon oxide. The floating metal is defined by the fifth lithography step and wet etched.

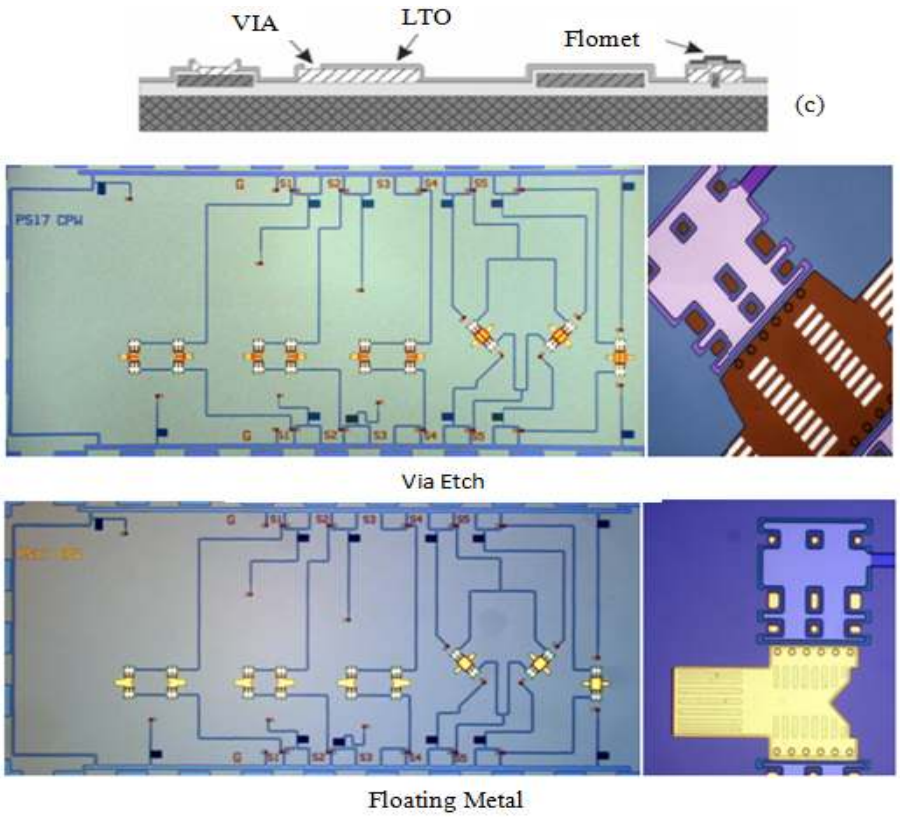


Fig. 6.1: (c) Process flow shows the LTO deposition, via opening and floating metal deposition. The images shows the via etch and the floating metal etch.

Photoresist from Fujifilm was chosen as sacrificial layer (spacer) for the fabrication of suspended movable membranes and air bridges, because it can be easily removed by oxygen plasma. The drawback is that only a partial planarization is obtained. After the sixth lithography to define the spacer, the resist is backed at 200°C, a temperature much higher than the usual one, in order to round the edges to improve step coverage as shown in the Fig. 6.1(d).

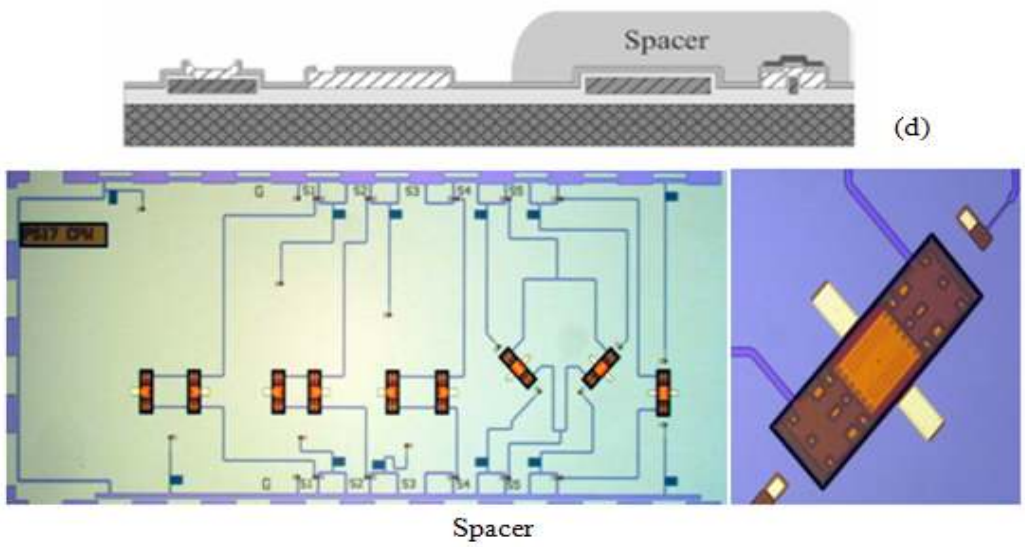


Fig. 6.1 :(d) Process flow shows the spacer deposition and backing. The Image shows the spacer image after the fabrication step.

After this treatment the resist is not dissolved by the solvents used in the next steps and, further lithography steps can be performed without damaging the spacer. A conductive seed layer for the electroplating process is then evaporated all over the wafer. This layer is composed of 2.5 nm of Cr, for adhesion to substrate, 25 nm of Au as conductive layer and a sacrificial top layer of 2 nm of Cr, to increase the adhesion of the photoresist mask during electroplating. In the seventh lithography step the pattern of the first Au film is defined by using a 6 µm thick layer of positive resist. After wet etching of the top Cr layer, 1.8µm thick Au layer, the so-called bridge layer, is electroplated by using cyanide based chemistry as shown in Fig. 6.1(e).

The deposition parameters have been chosen in order to obtain a slightly tensile residual stress. After photo-resist removal, the eighth lithography step defines the pattern of a second thicker of 3.5µm Au layer called CPW, which is also grown by electroplating. The thinner bridge layer is used mainly to fabricate the suspended and movable structures while low resistance lines, ground areas and the anchor points of movable structures are fabricated by superimposing both the gold layers. Frequently, CPW layer is deposited over selected

areas of movable bridges in order to have stiffer parts that move rigidly while deformation is localized on thinner suspension spring legs.

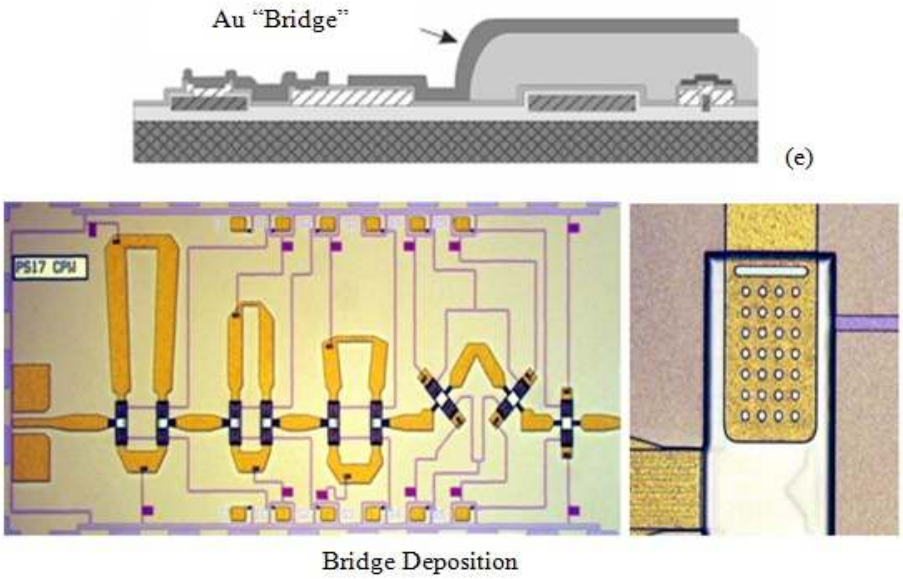
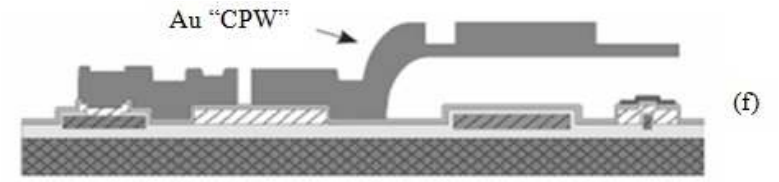
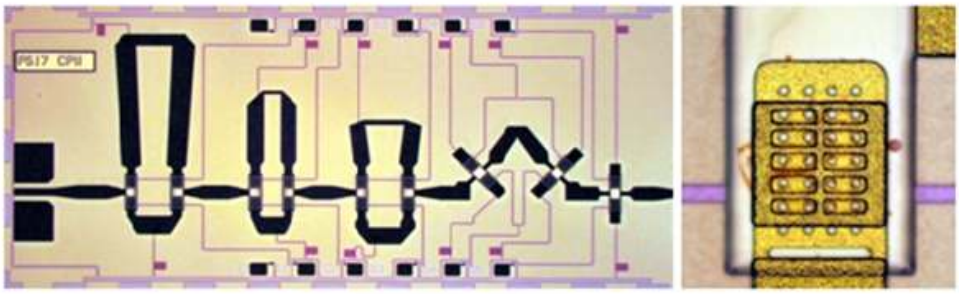


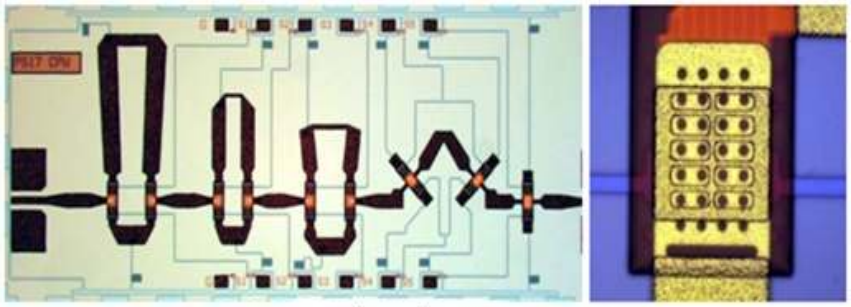
Fig. 6.1 :(e) Process flow shows the seed layer and first Au/Bridge" electroplating and the Image of the bridge deposition is shown.

In order to control the contact force on ohmic switches the central part of the movable membrane is made of a thick bridge plus CPW Au layer. Cantilevers tips or lateral wings on clamped-clamped beams are designed using only thinner bridge layer. The seed layer is removed by wet etching and a gold sintering at 190°C is performed to increase the gold adhesion to substrate and the bond ability of pads for external connections. In addition this step leads to a more homogeneous and reproducible (tensile) stress value in the gold membranes. The last process step is the release of suspended structures by removal of sacrificial resist with oxygen plasma as shown in the Fig. 6.1(f).The process temperature and the etching parameters were optimized in order to reduce the structure deformations induced by stress and stress gradient along the thickness of films.

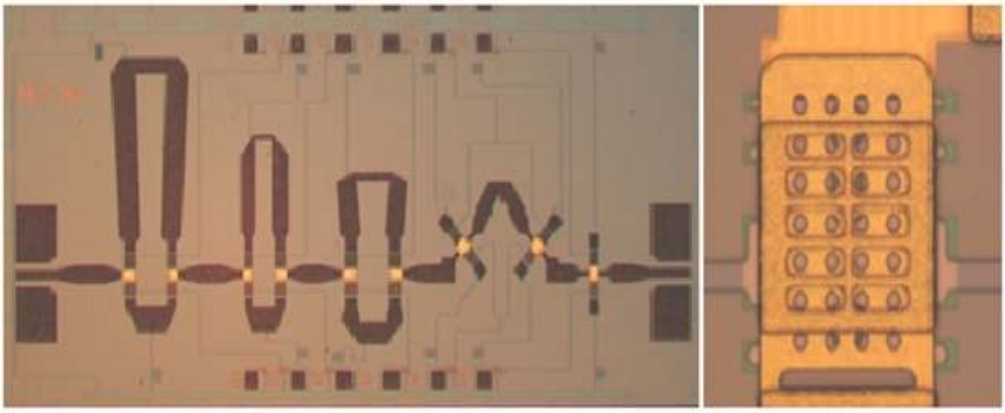




CPW Deposition



Final Pre-release



Final Structure

Fig. 6.1: (f) Process flow shows the second Au /CPW electroplating and release of suspended structures. The Image shows the die with zoomed view of the CPW Deposition, final Pre-release and final structure.

6.2 In- process Inspection

In-process inspection was carried out at various levels of process steps in order to verify the fabrication. Table 6.1 presents the various in-process parameters like oxide thickness, multi metal sheet resistance, poly step height and Flomet thickness etc. measured during the device fabrication with their mean, deviation and the measurement method.

Table 6.1: Parameters measured on the Test Wafers of the Batch

Parameter	Unit	Mean	1σ	Measurement Method
Thermal Oxide thickness	nm	1032	4	Interferometer
Poly silicon thickness	nm	633	8	Interferometer
Polysilicon Sheet Resistance	Ohm/sq	1599	41	4 point probe
TEOS Thickness	nm	308	3	Interferometer
Field Oxide + TEOS	nm	1308	4	Interferometer
Polysilicon + TEOS Steps height 630	nm	692	17	Stylus Profiler
Multi-metal Sheet Resistance	Ohm/sq	0.07875	0.016	4 point probe
Residual oxide after metal dry etch	nm	1219	7	Interferometer
LTO Thickness	nm	114	7	Interferometer
Multi-metal step height post LTO	nm	674	11	Stylus Profiler
Poly step height LTO (630nm)	nm	653	13	Stylus Profiler
Flomet Thickness Cr/Au(5/150)	nm	166	3	Stylus Profiler

6.3 Test Structures and Inspection results

Test structures layout was included in the wafer layout with one horizontal array of tests structures and four small vertical arrays as shown in Fig. 6.2. Every vertical array was formed by 3 test patterns i.e. test strip, electromechanical test structure and mechanical test pattern while the long horizontal array contains 16 electrical test strip, 10 electromechanical test structures and 4 mechanical test patterns.

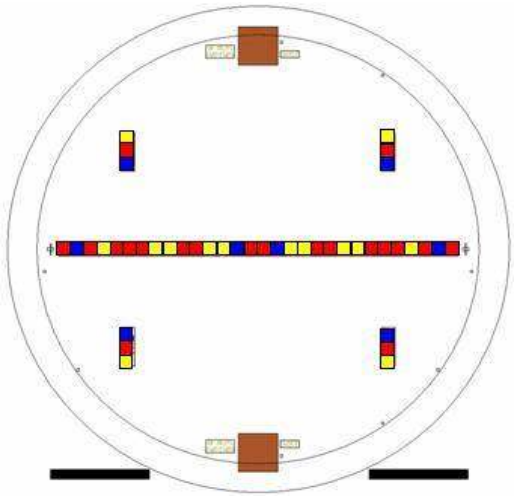


Fig. 6.2: Scheme of the test structures across the wafer with the position of parametric test pattern (red squares), thickness test pattern (blue squares) and electromechanical test structures (yellow squares).

6.3.1 Spacer Thickness

The spacer thickness was measured with two methods by using the interferometer and a mechanical stylus profiler before and after spacer deposition. Planarization of the resist occurred to some extent. Both the spacer and LTO profiles have been measured with a stylus profiler. Spacer profiles have been measured after seed layer deposition. Table 6.2 shows the spacer measured spacer values by the two methods. While the Fig.6.3 shows the spacer thickness profile

Table 6.2: Spacer Thickness. All values in µm

Nominal Value	Interferometer	Profiler	Profiler (On Poly)
3.0	2.629±0.032	2.690	2.393

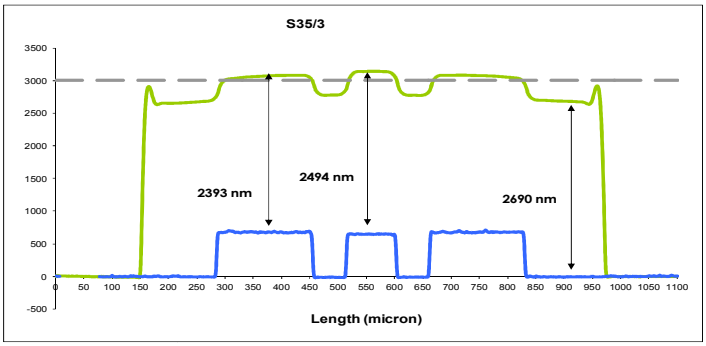


Fig.6.3: Spacer thickness profile on device wafer. Nominal value = 3000 nm.

6.3.2 Gold Thickness

Gold thickness has been measured by means of a stylus profiler on dedicated test structures. The deposition conditions are current intensity 2mA/cm^2 with 20 and 28 minutes of deposition time for bridge and CPW layers respectively. Figure 6.4 shows the image of the fabricated patterns on which measurement was carried out. Table 6.3 presents the measured values of the all the three process depositions i.e. BRIDGE, CPW and BRIDGE + CPW. Data are averaged over 5 values.

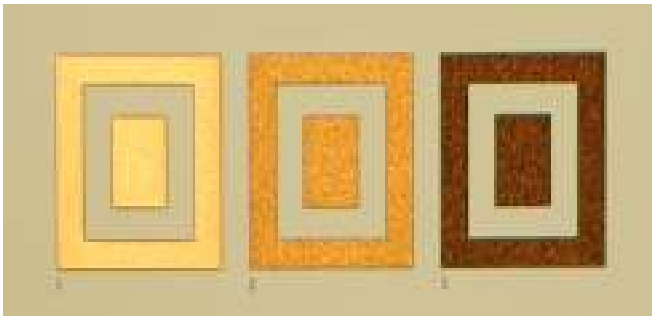


Fig. 6.4: Test pattern for gold thickness measurement of the BRIDGE (pale yellow -1), CPW (gold-yellow - 2) and BRIDGE+CPW (brown -3) gold layers.

Table 6.3: Gold layer thickness values for BRIDGE, CPW and BRIDGE + CPW.

All values in μm.

BRIDGE	CPW	BRIDGE+CPW
2.20±0.06	2.91±0.29	5.95±0.23
2.07±0.16	2.92±0.14	5.79±0.26
2.11±0.10	2.81±0.20	5.68±0.22

6.3.3 Electrical Test Patterns

The parametric test structures have been measured by means of an automatic Wafer Prober EG2001X equipped with switching matrix B2200A, a HP5270 for I-V measurements and a HP 4284A/4285A for CV measurements. One of the electrical test patterns is shown in Fig. 6.5. The pad dimensions are 90x90μm^2.

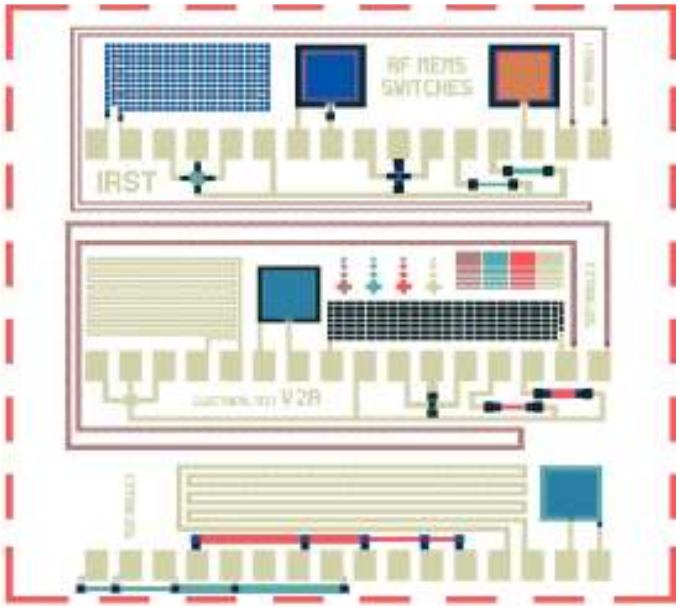


Fig.6.5: Electrical Test Pattern.

The test pattern has different test structures that allow measuring the relevant electrical parameters of all layers and structures. All capacitors are 200×200 μm^2. Contacts are 4×4

μm^2 for contact chains and 10×10 μm^2 for contact resistances. The summary of measurements of various electrical parameters is shown in the Table 6.4.

Table 6.4: Measured Electrical Test Parameter Presented with the Mean Values

Value	Unit	Mean Values
Poly-silicon sheet resistance	Ω/□	1522±42
Multi-metal sheet resistance	Ω/□	0.0754±0.0009
Au BRIDGE sheet resistance	Ω/□	0.0119±0.0004
Poly-Si/multi-metal. DC contact resistance	Ω	13±2
Multi-metal /Au DC contact resistance	Ω	0.56±0.28
Poly-Si/multi-metal contact chain resistance	Ω	3217±354
Multi-metal/Au DC contact chain resistance	Ω	17±17
Poly-Si/Au capacitance	pF	14.0±0.2
Poly-Si/multilayer capacitance	pF	5.4±0.2
Multilayer/Au capacitance	pF	15.6±1.0
LTO thick. (Multilayer/Au capacitance)	nm	89±5
TEOS thick. (Poly-Si/TiN capacitance)	nm	258±7
% of measurable test patterns		100%

6.3.4 Electromechanical Tests Structures

The electromechanical test structures included in the layout have been designed and measured by the automatic wafer prober. The structures included consist of two arrays of 5 bridges not surrounded by coplanar waveguide ground plane. This makes them suitable for CV measurements. Figure 6.6 shows one of these electromechanical test structures.

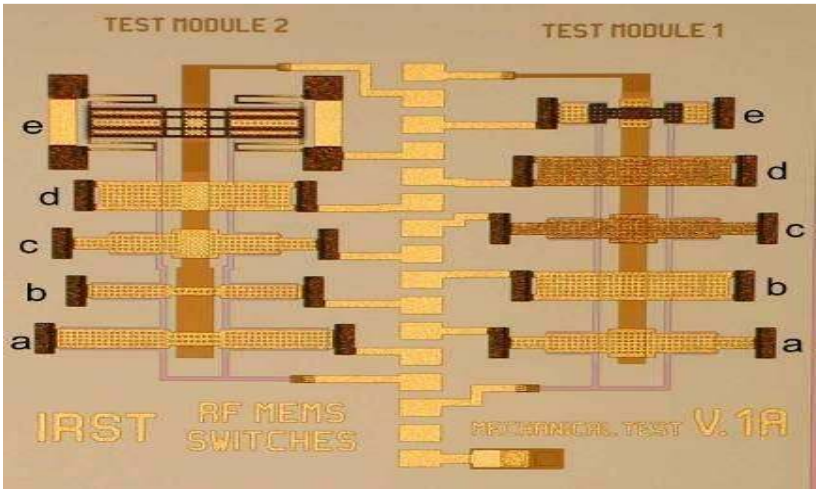
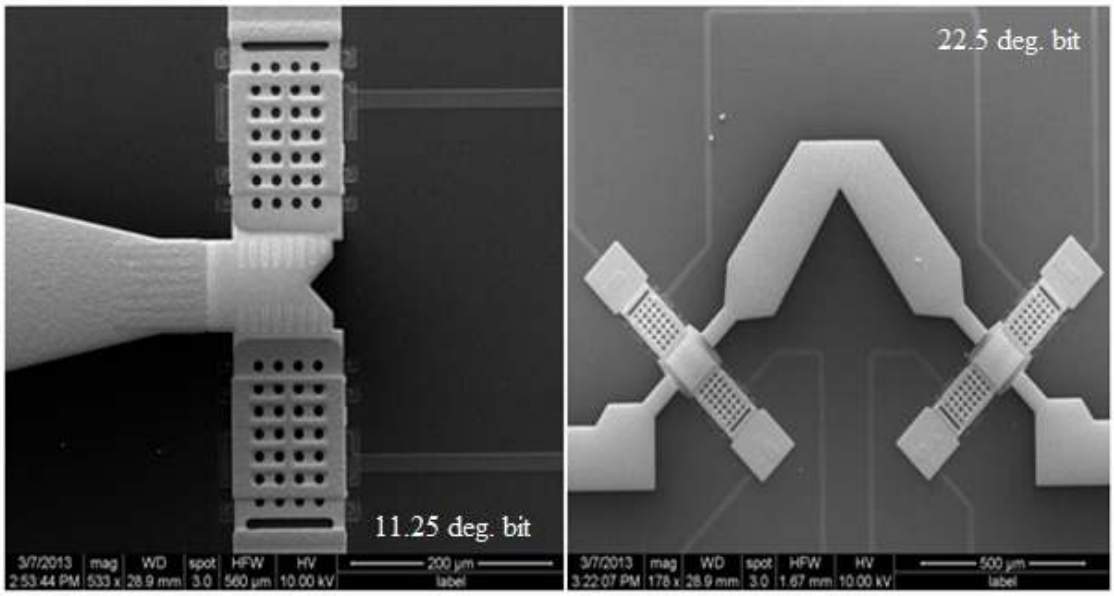


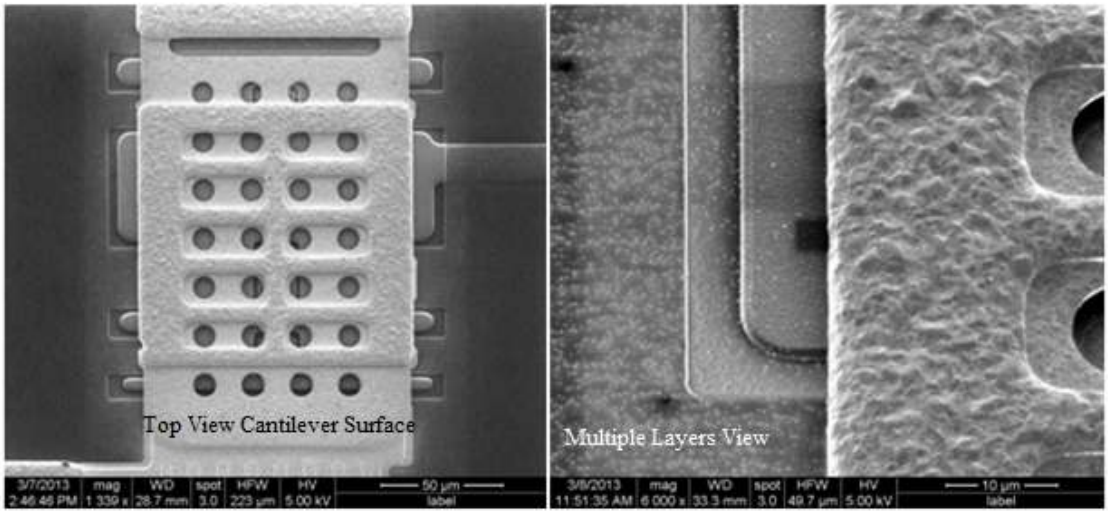
Fig. 6.6: Electromechanical Test Structure pattern.

6.3.5 SEM Inspections

Scanning electron microscope was used to carry out the inspections of the surface topography. Various types of views and sections were taken up for SEM inspection. Figure 6.7 (a-d) shows the various sections of the fabricated phase shifter.



(a) (b)



(c) (d)

Fig. 6.7 (a) and (b) shows the complete view of the 11.25° and 22.5° bit respectively while (c) shows the Zoomed view of cantilever part and the (d) shows the zoomed view of different layers.

Summary

This chapter has presented the detailed layer wise fabrication process, cross sectional views and the Images at every step. The thickness measurement was carried out using tools like profiler and interferometer. The SEM was used for surface evaluations. Very exhaustive electrical measurements were performed at every step for the resistance and the capacitance to verify the process and have been found in agreement with the expected results.

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CHAPTER 7

On-Wafer RF Characterization of CPW Single bits and 5-bit Phase Shifter

As explained earlier in chapter 5, via less CPW transitions were incorporated to the microstrip design to evaluate the on wafer performance of the single bits and the 5-bit integrated phase shifter device. The on-wafer RF performance characterization is very significant from design verification point of view and it requires accurate test methodology and set up to evaluate the device performance. This chapter presents the test set up, on-wafer RF characterization of the singular bits and integrated phase shifter using TRL cal kit fabricated on the wafer and the test methodology adopted.

7.1 Test set up and fabricated wafer layout

RF Measurements have been performed at wafer segment level by using TRL on-wafer calibration kit with PNA E8363C vector network analyzer and a voltage source. The measurement test setup is shown in Fig. 7.1. The device is accessed by means of a probe station, represented by the grey plate containing the DUT. The DC probes touching the control pads have been connected to the Agilent power supply E3649A, while the RF probes touching the RF input and output are connected to the PNA Vector network Analyzer. The cascade 200μm GSG probes have been used. The VNA to RF probes have been connected via RF cables having frequency capability up to 40GHz. GND signal is connected to 0V imposed by the instrument. The VNA has been accessed through PC using the software

program. All instruments i.e. PNA and Voltage Source etc. probe chuck and every metal support have been connected to a common and very stable electrical GND to ensure the accurate measurements. A partial layout and image of the part of the fabricated wafer containing the CPW phase shifter device and TRL calibration kit are shown in the Fig. 7.2 (a) and (b).

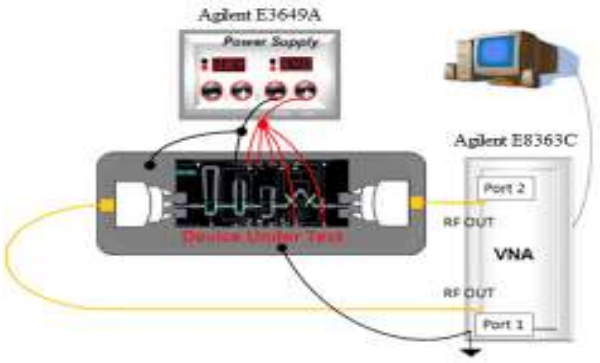


Fig. 7.1: Test Setup for on wafer probe characterization of single bits and phase shifter with CPW interconnections.

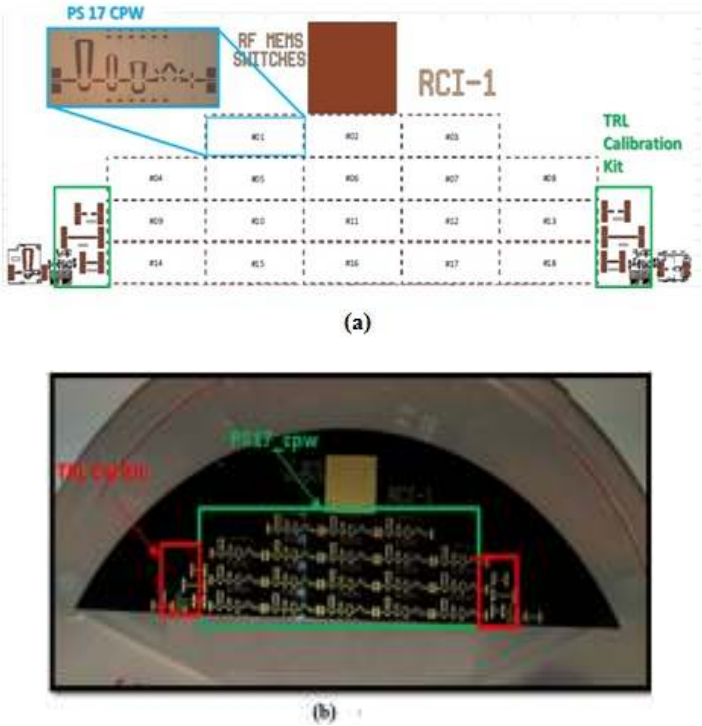


Fig. 7.2: (a) Partial layout and (b) part of the fabricated wafer.

7.2 On-wafer TRL Calibration Kit

The Image and RF performance of the TRL calibration kit is shown in Fig. 7.3 (a) and (b) respectively. The TRL calibration kit allows to move the measurement reference plane so that it does not include in the measurements, the loss contribution of the via-less coplanar-to-microstrip transition. TRL on-wafer calibration has been used to measure the phase shifter single bits as well as of the 5-bit device with CPW transition in the phase shifter frequency band of 16-18 GHz. The TRL calibration kit presents the following parameters as return loss better than 40dB and average insertion loss 0.25dB in 16-18 GHz frequency band.

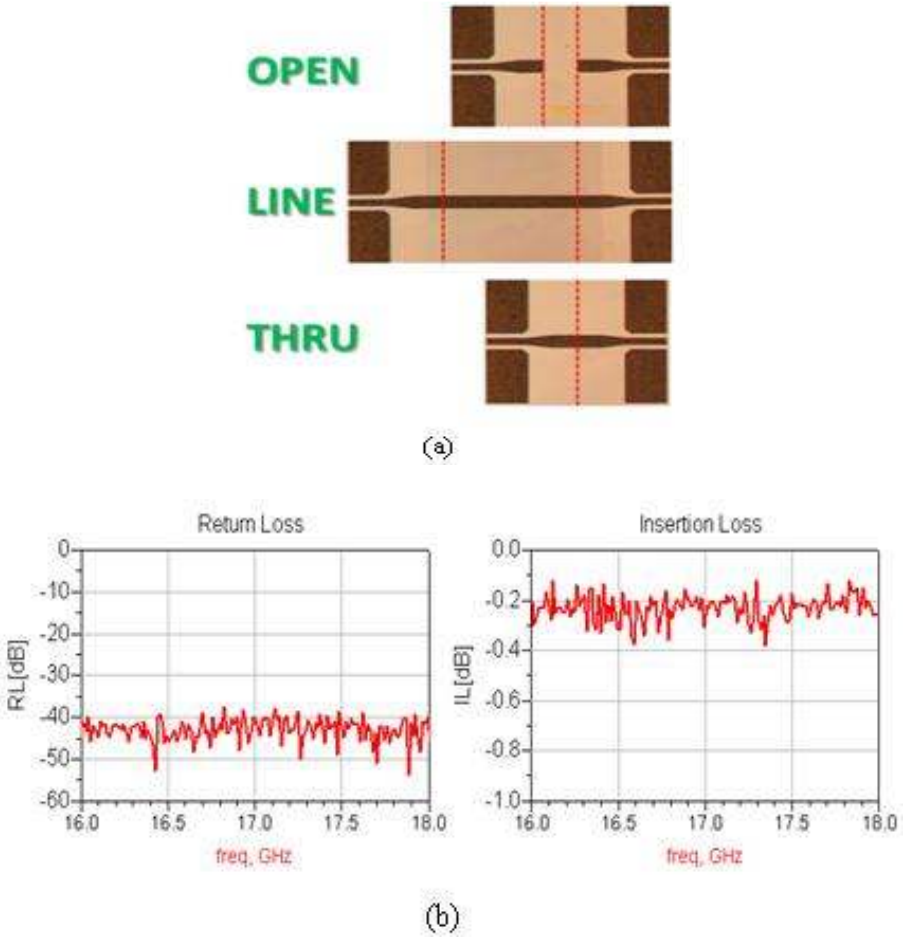


Fig. 7.3: (a) Image of TRL calibration kit with reference planes (red dot line) and (b) LINE measured Return Loss and Insertion Loss.

7.3 RF Performance of the Ohmic series SPST switch

Series Ohmic MEMS cantilever switch has been the constituting element of the proposed phase shifter. This switch acts as switching element of the developed phase shifter. The Image of the fabricated device in series with respect to a 1.8mm long coplanar line is presented in Fig. 7.4 (a) with the measured RF performance. It shows insertion loss better than 0.6 dB and return loss better than 24dB from DC up to 20GHz. The actuation voltage is in the range of 38-47V and consequently 60V voltage ensures the complete actuation of the switch. The performance has been compared with the performance of the same switch actuated by design, to evaluate the impact of the Switch contact resistance. Indeed the "actuated by design" switch shows 0 contact resistance and can be used as a reference line. Figure 7.4(b) shows the comparison of the two performances showing negligible impact of the MEMS contact resistance on the performance of a single switch. By fitting the measured performance with equivalent circuit, on-state contact resistance R_{on} better than 0.9 Ohm and off-state capacitance C_{off} of about 10fF were extrapolated. These values are fully in-line with the expected values of the MEMS series ohmic switch.

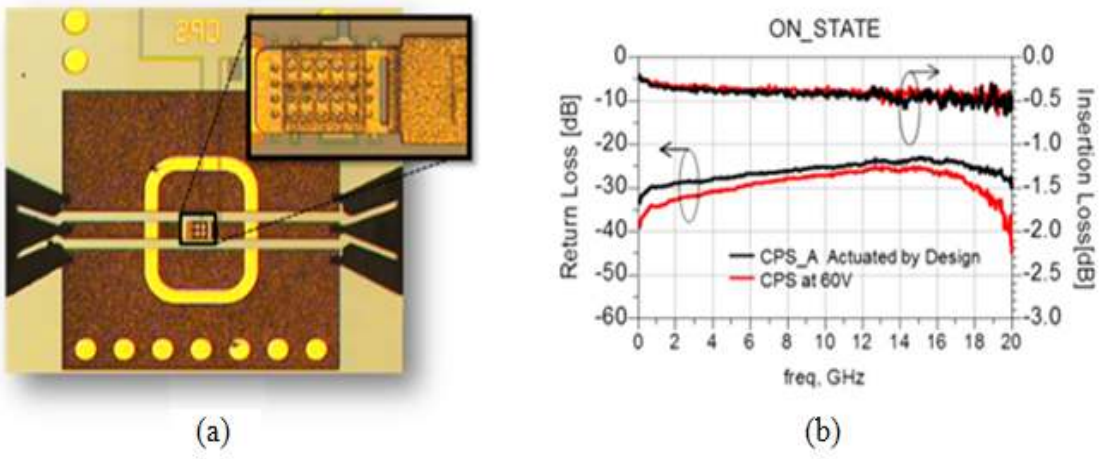


Fig. 7.4: (a) Image of MEMS SPST cantilever in series with a 1.8mm long coplanar line and (b) measured isolation at 0V in comparison with the ideal switch (switch actuated by design).

7.4 Single Bit RF Performance

The single bits have been measured as per the RF test set up described in section 7.1 and TRL on-wafer calibration in section 7.2. The image of the fabricated bits and results are shown in Fig. 7.5 to 7.9 for respective bits.

7.4.1 Measured Results: 180° phase bit 1

On-wafer measurements for 180° phase bit 1 show that the return loss is better than 14dB and 26dB while average insertion loss is 1.5dB and 1.2 dB for long path and short path respectively as shown in Table 7.1.

Table 7.1: On-wafer measurements for 180° phase bit 1.

Parameter	Short Path	Long Path
Return loss (dB)	26	14
Average Insertion loss (dB)	1.2	1.5

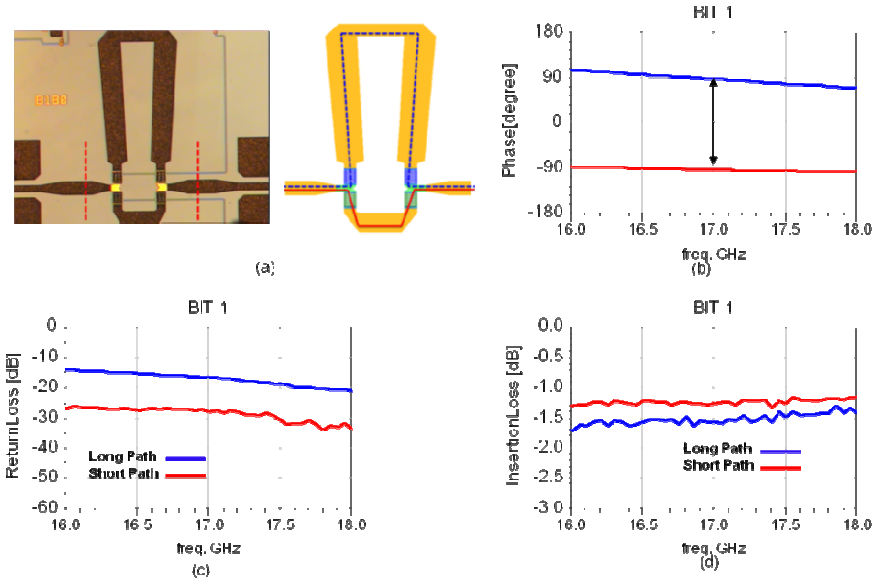


Fig. 7.5: (a) Image-layout, (b) phase shift, (c) return and (d) insertion loss of Bit 1 (180^{o}).

7.4.2 Measured Results: 90° phase bit 2

On-wafer measurements for 90° phase bit 2 shows that the return loss is better than 20dB and 31dB while average insertion loss is 1.2dB and 1.3 dB for long path and short path respectively as shown in Table 7.2.

Table 7.2: On-wafer measurements for 90° phase bit 2.

Parameter	Short Path	Long Path
Return loss (dB)	31	20
Average Insertion loss (dB)	1.3	1.2

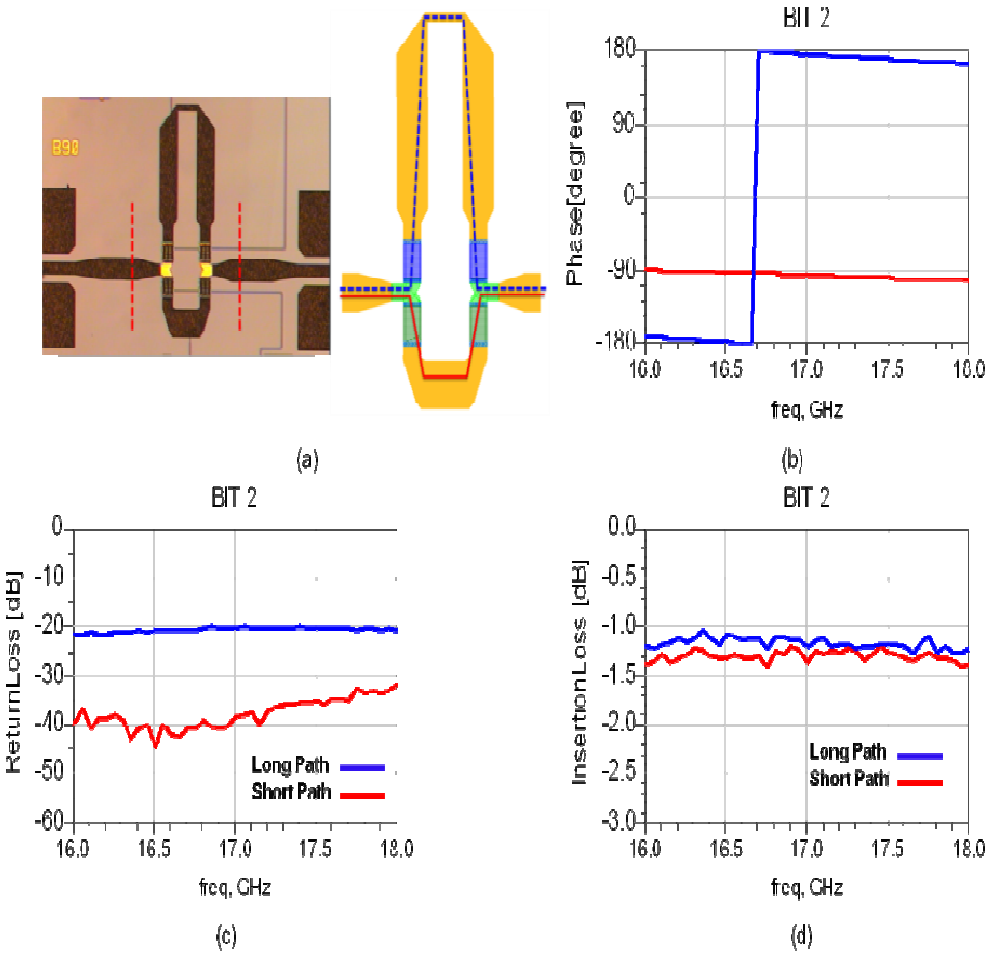


Fig. 7.6: (a) Image-layout, (b) phase shift, (c) return and (d) insertion loss of Bit 2 (90°).

7.4.3 Measured Results: 45° phase bit 3

On-wafer measurements for 45° phase bit 3 shows that the return loss is better than 20dB and 31dB while average insertion loss is 1.15dB and 1.3 dB for long path and short path respectively as shown in Table 7.3.

Table 7.3: On-wafer measurements for 45° phase bit 3.

Parameter	Short Path	Long Path
Return loss (dB)	31	24
Average Insertion loss (dB)	1.3	1.15

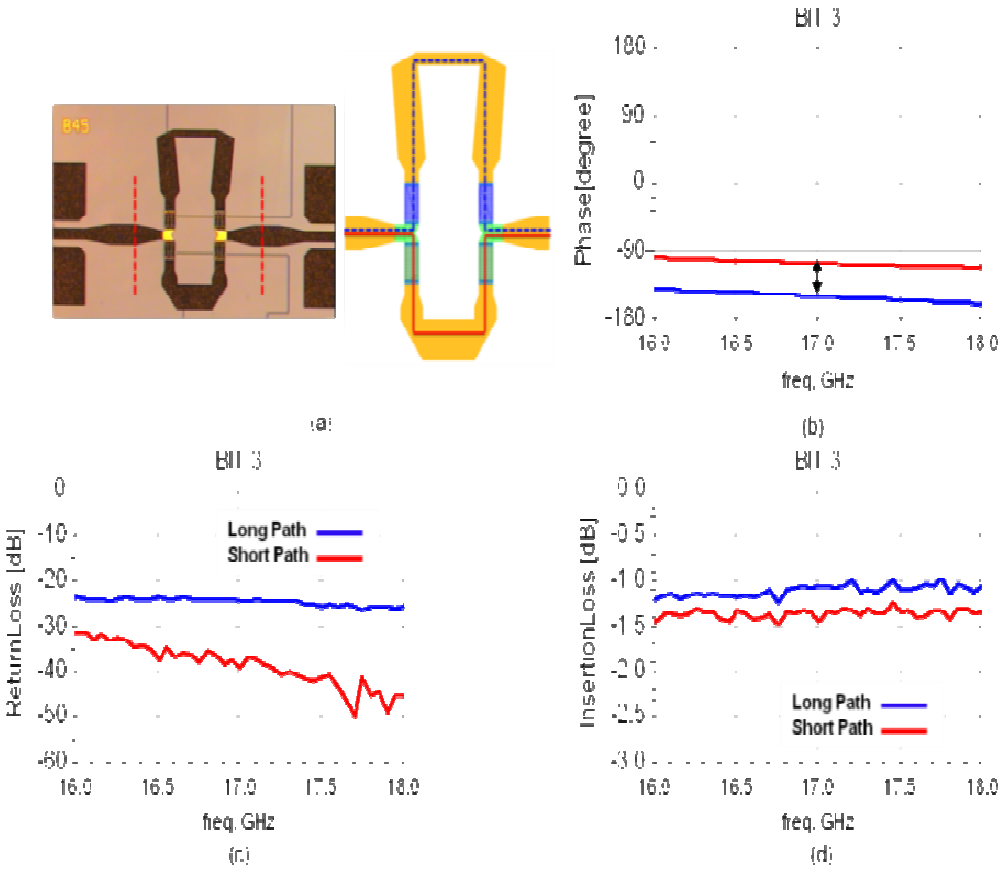


Fig. 7.7: (a) Image-layout, (b) phase shift, (c) return and (d) insertion loss of Bit 3 (45°).

7.4.4 Measured Results: 22.5° phase bit

On-wafer measurements for 22.5° phase bit 4 shows that the return loss is better than 24dB and 22dB while average insertion loss is 1.1dB and 0.9 dB for long path and short path respectively as shown in Table 7.4.

Table 7.4: On-wafer measurements for 22.5° phase bit 4.

Parameter	Short Path	Long Path
Return loss (dB)	22	24
Average Insertion loss (dB)	0.9	1.1

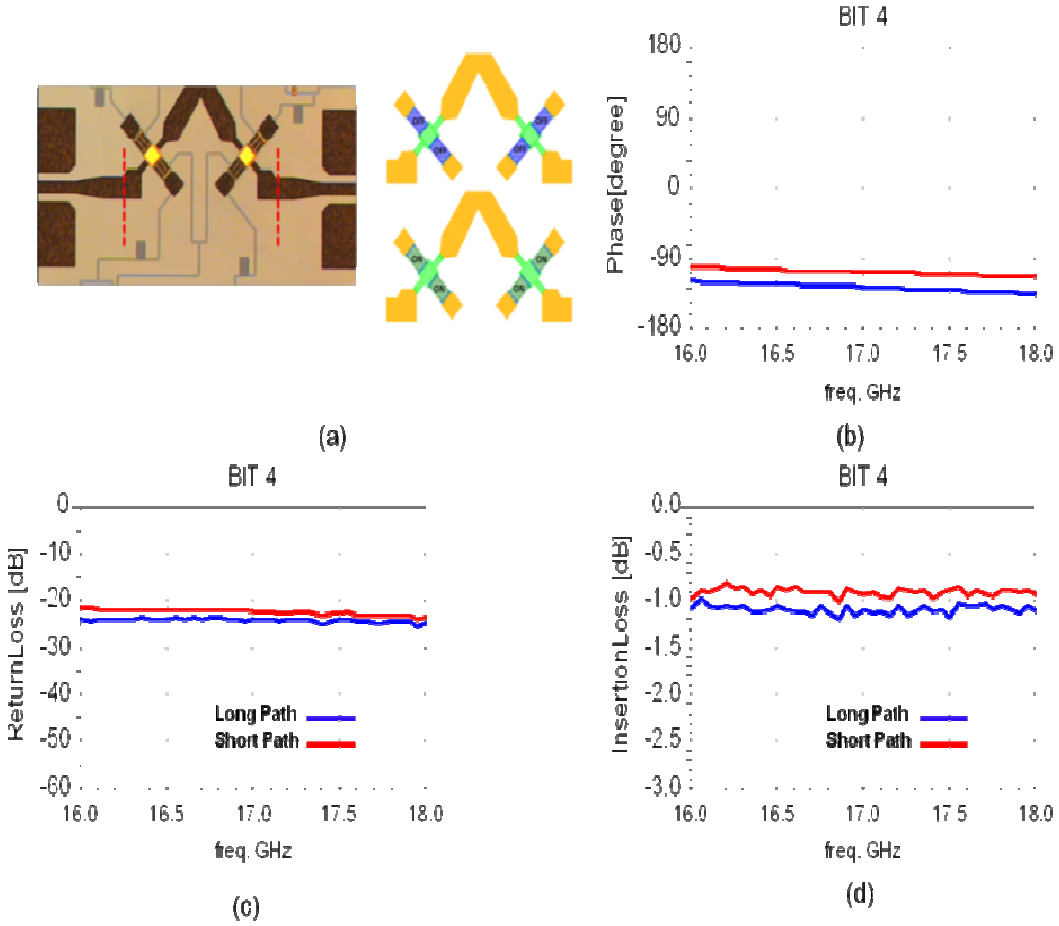


Fig. 7.8: (a) Image-layout, (b) phase shift, (c) return and (d) insertion loss of Bit 4 (22.5°).

7.4.5 Measured Results: 11.25° phase bit

On-wafer measurements for 11.25° phase bit 5 shows that the return loss is better than 27.5dB and 18dB while average insertion loss is 0.55dB and 0.55 dB for long path and short path respectively as shown in Table 7.5.

Table 7.5: On-wafer measurements for 11.25° phase bit 5.

Parameter	Short Path	Long Path
Return loss (dB)	18	27.5
Average Insertion loss (dB)	0.55	0.55

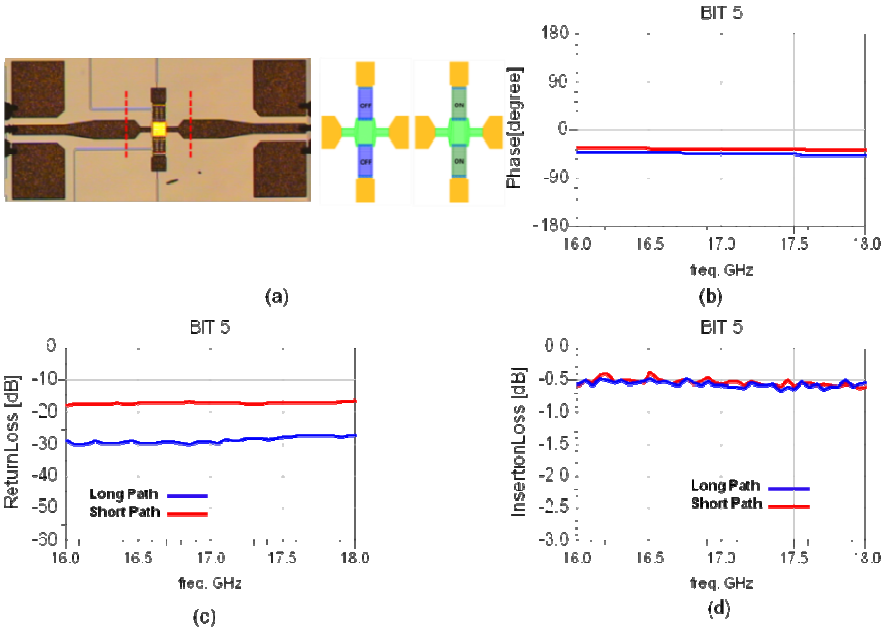


Fig. 7.9: (a) Image-layout, (b) phase shift, (c) return and (d) insertion loss of Bit 5 (11.25^{o}).

Table 7.6 shows the summary of the phase error measured bit wise for the individual bits. The maximum phase error -1.84° was observed for the 22.5° loaded line bit while 180^{0} bit was measured with minimum phase error with -0.08° phase error. The phase error observed in the performance is well within the tolerance to the design.

Table 7.6: Summary of the achieved phase error of the individual phase bits.

Bit #	*Bit Type*	*Theoretical Phase Shift [deg]*	*Phase Shift Error [deg]*
1	Switched Line	180°	-0.08°
2	Switched Line	90°	-1.37°
3	Switched Line	45°	-1.06°
4	Loaded Line	22.5°	-1.84°
5	Loaded Line	11.25°	-1.44°

7.5 5-bit Phase Shifter Measurement and Results

The characterization of a 5-bit phase shifter is a complex work and requires a dedicated set up as it is not possible to bias all the dc pads by the probes at a time without dc probe cards. A dc probe card was designed as per the pad pitch and other dimensional details. The frequency band of 16-18 GHz was selected with 0dBm as the input power to the phase shifter. The 5-bit phase shifter RF measurement has been performed via 200µm pitch GSG microprobes using Agilent E8363C PNA vector analyzer and a voltage source. The device was accessed by means of a probe station. As shown in the Fig. 7.10, there are 12 actuation pads present and are shown on upper and lower side of the die Image. These have been named as S1, S2, S3, S4, S5 and two ground pads G. Both the ground pads have been short circuited by design internally. The pads S1 to S3 drive the bits 1 to 3 respectively (S1 →180° bit, S2 → 90° bit, S3 → 45° bit). Since the first three bits are in a switches line topology these were polarized to select the shorter path or the longer path and thus obtain the phase shift associated to the particular bit. On the contrary the two other pad i.e. S4 and S5 pads were polarized either low or high at the same time to obtain 22.5° and 11.25° phase shift corresponding to the 4^{th} bit and 5^{th} bit respectively. The yellow line path and labelling on the

Fig. 7.10 shows the total phase shift as 292.5°. In this example, first two bits have taken the longer path while third bit has followed the shorter path in the switched line configuration as described. The fourth bit was polarized for loading while fifth bit was not actuated and provided the reference phase only. The following polarization scheme has been adopted during RF characterization.

i. Range of Freq = 16-18 GHz

ii. Central frequency = 17GHz

iii. Input Power = 0dBm

iv. Driving Voltage = 0V (state 0) - 60V (state 1)

Figure 7.11 shows the corresponding binary format to achieve the above description. The 0 state means 0V and 1 state represent 60V for polarization. This binary format shows the binary information of the switch in up and down position.

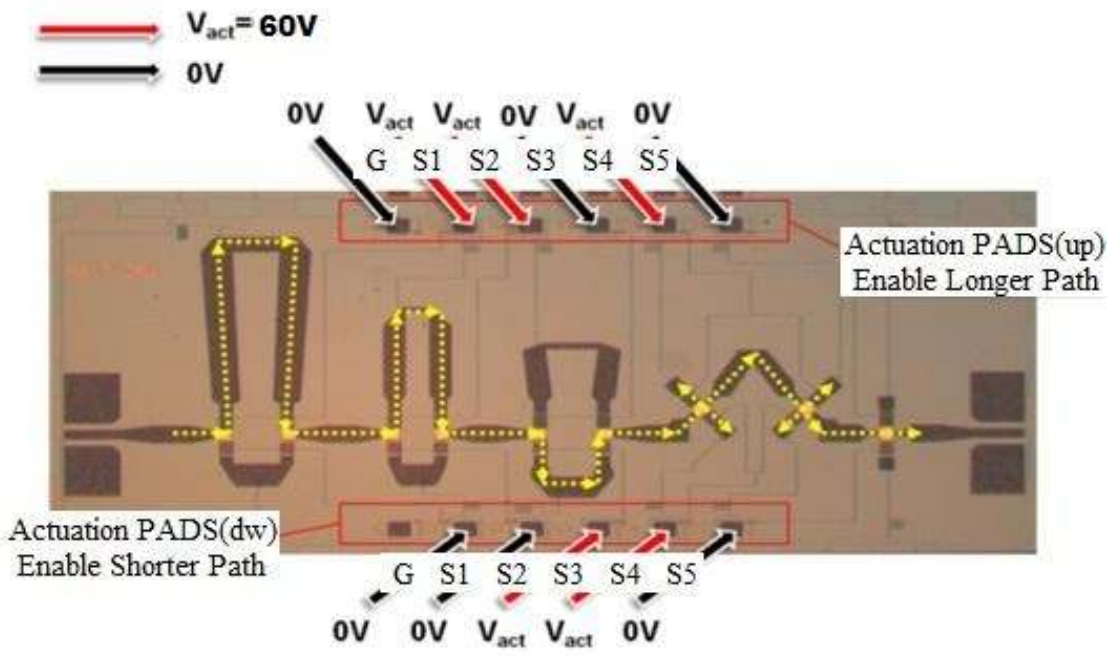


Fig.7.10: Image of fabricated phase shifter with an example of the polarization on dc bias pads of the device to achieve the Phase shift of 292.5°.

Binary format				
10	10	01	11	00

Actuation PADS									
S1(up)	S1(dw)	S2(up)	S2(dw)	S3 (up)	S3 (dw)	S4(up)	S4 (dw)	S5 (up)	S5 (dw)
1	0	1	0	0	1	1	1	0	0

Fig. 7.11: An example of binary format (10 10 01 11 00), (Phase shift= 180° + 90° + 22.5°= 292.5°).

The measured RF results obtained for the monolithic 5-bit MEMS phase shifter have been shown in Fig. 7.12 (a-d). The Return loss better than 12dB and average insertion loss better than 3.21dB have been measured for the 32 states in the 16-18GHz frequency band. The minimum and maximum insertion loss is 2.15dB and 3.84dB respectively. The average return loss is 20.64dB. The average Phase Shift Error has been 1.52 degrees. The worst case phase shift error was observed as 1.84 degrees over the 32 states.

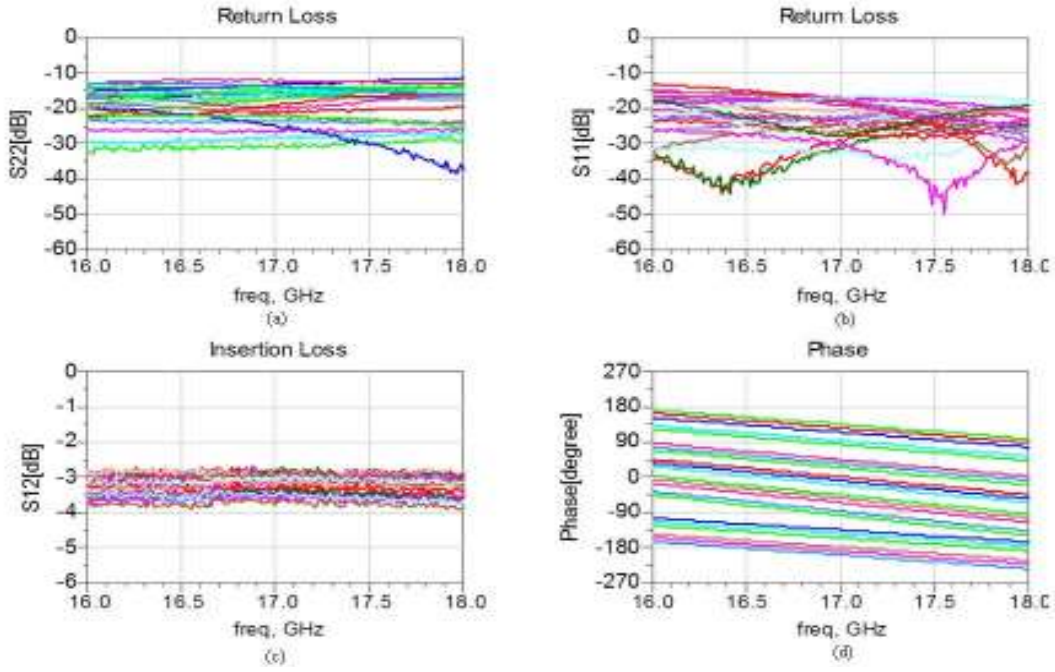


Fig. 7.12: Measured performance of the 5-bit MEMS phase shifter for 32 states (a) output return loss, (b) input return loss, (c) insertion loss and (d) Phase shift.

Summary

The on-wafer RF characterization of the single bits has shown the phase shift error well within 2 degrees however insertion loss of singular bits has been higher than the expected. This could be due to the via less transition. In case of integrated 5-bit device, the device has not shown that much higher insertion loss. It is very close to the simulated one and just higher by one bit as expected due to the non zero ohmic contact resistance.

*****

CHAPTER 8

5-bit Microstrip Phase Shifter Characterization on Jig

The field application of phase shifter requires it to be in the microstrip version so as this can be implemented as a drop-in component along with other devices like MMICs developed with GaAs technology. The subsystems namely T/R modules are the one which needs them in large numbers for their ultimate application in the active electronically steerable antennas. For the above cited reason it is absolute necessary to develop and test it in the microstrip configuration. This chapter presents the design of test jig and control board along with the GUI interface. The RF test results of the phase shifter over 32 states in 16-18GHz frequency band are also presented in this section.

8.1 MEMS Phase Shifter Test Jig Design

In order to verify the performance of the microstrip version before incorporating into the system it was required to evaluate its performance. The complete phase shifter was configured for mounting on to a carrier substrate. This was designed as a connectorized version having two possible options. One with the SMA connectors as shown in the Fig. 8.1(a), requires a welding process to bond the RF line with the input and output connector which makes the test jig limited to one device testing. The second one is as shown in the Fig. 8(b) with end launch type connector was designed and finalised as it can be reused for multiple evaluations. The base substrate was taken as Rogers 6202 plastic laminate provided with a metallic support at the bottom. The dc connector is provided on the top to connect a cable for biasing the phase shifter as per binary format for complete 32 states evaluation.

Control circuitry hardware was designed then connected to provide software and PC interface to control the 12 dc signals necessary to drive the 5 bit phase shifter.

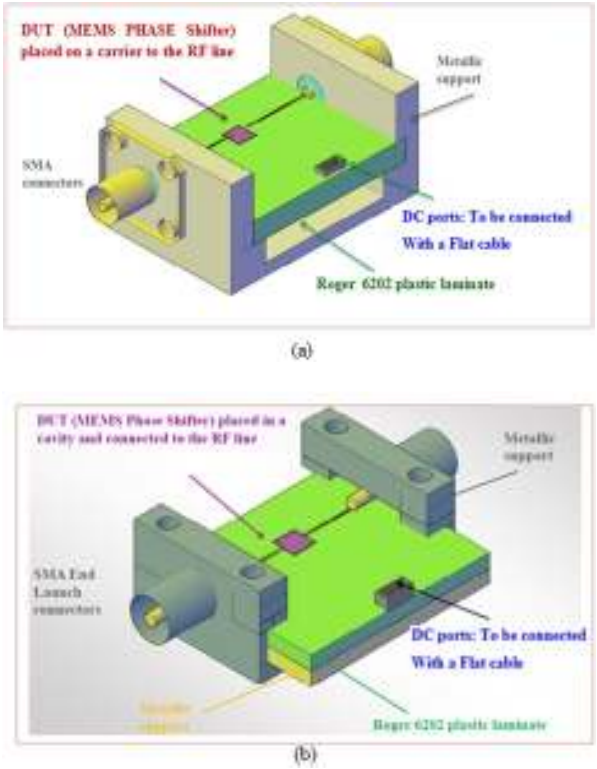


Fig. 8.1: Test jig design (a) SMA connectors and (b) end launch connectors.

The microstrip version for jig level testing was designed with a modified layout as shown in the Fig. 8.2. The L-C sections have been developed to compensate the parasitic effects of jig mounting. These matching sections have been designed on the die itself.

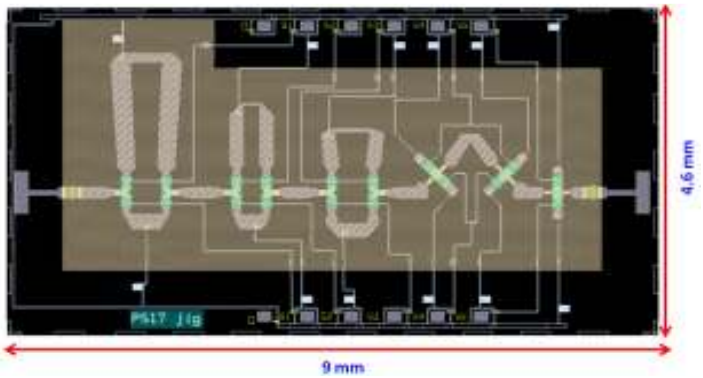


Fig.8.2: Microstrip layout of test jig version.

The interface bonding requirements have been analyzed and multiple bond wires were designed and simulated. The detailed view along with the dimensional detail of the substrate, die height and bond wire lengths has been shown in the Fig. 8.3.

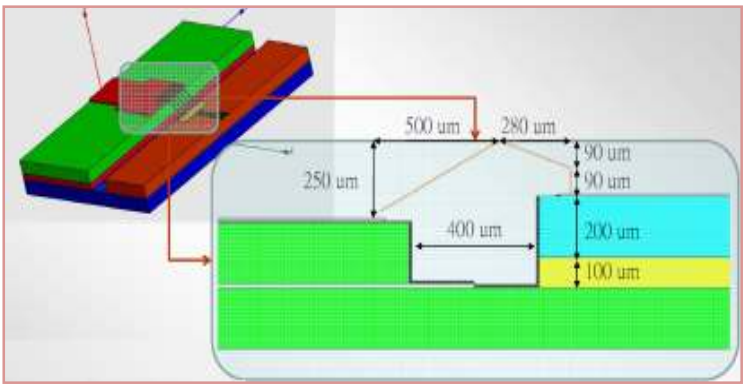
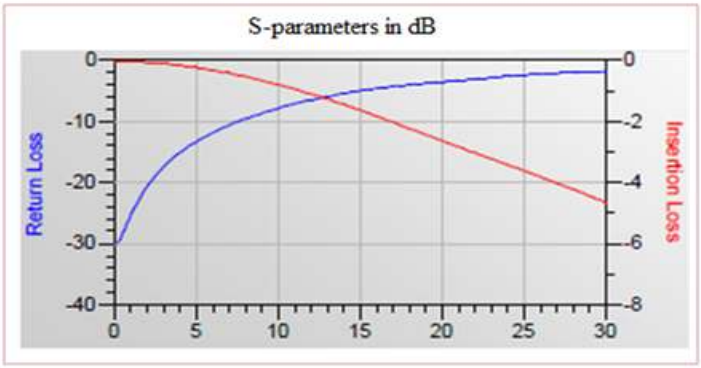
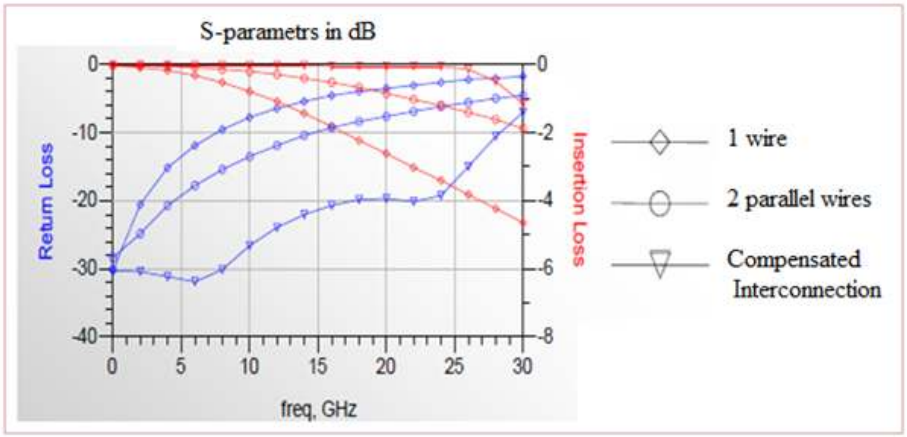


Fig. 8.3: Interface of the die with bond wire and substrate details.

The RF performance comparisons of the compensated and non-compensated RF interconnections are shown in the Fig. 8.4 (a) and (b). The non-compensated performance has degradation in both the insertion and return loss. The compensated interconnection have been optimized to minimize the effects of the mismatch introduced by highly inductive wire bonding and to obtain good return loss and low insertion loss even at high frequencies up to 25GHz which serves the aim of this study up to 18GHz. The simulation shows the satisfactory results after introduction of the compensation.



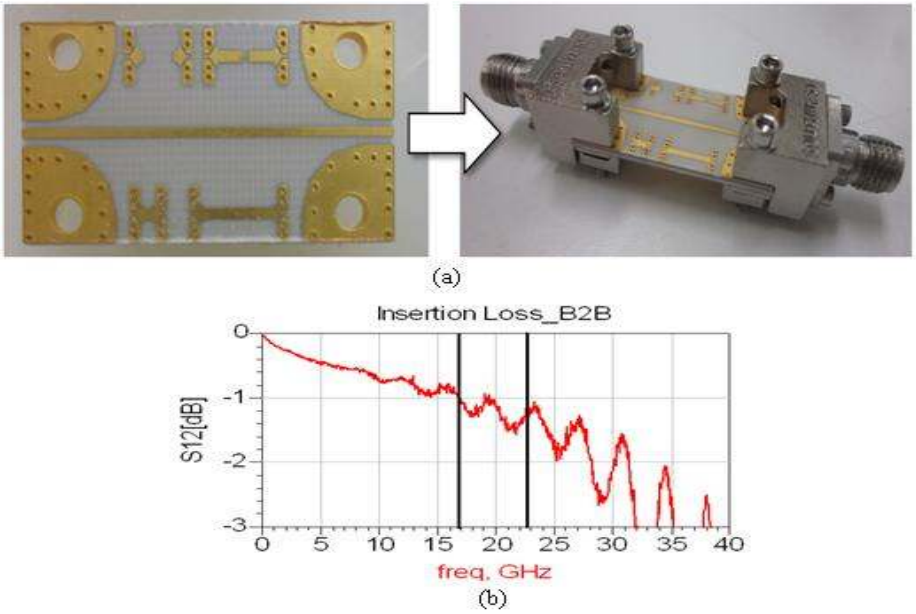
(a)



(b)

Fig.8.4: RF performances of the (a) non-compensated structure and (b) the compensated structure with the L-C section and the multiple bond wires.

The test jig evaluation for RF performance in terms of insertion loss without the phase shifter as shown in Fig. 8.5 (a) was carried out in order to accurately measure the insertion loss of the microstrip version phase shifter.



(a)

(b)

Fig.8.5: (a) RT duroid layout and its connectorized version while (b) shows the RF insertion loss of test jig over 0-40GHz frequency range.

The insertion loss of the RF measurement has been shown in the Fig. 8.5 (b) and observed as 1.35dB at 17GHz. The Image of the microstrip version fabricated for on jig testing has been shown in the Fig. 8.6.

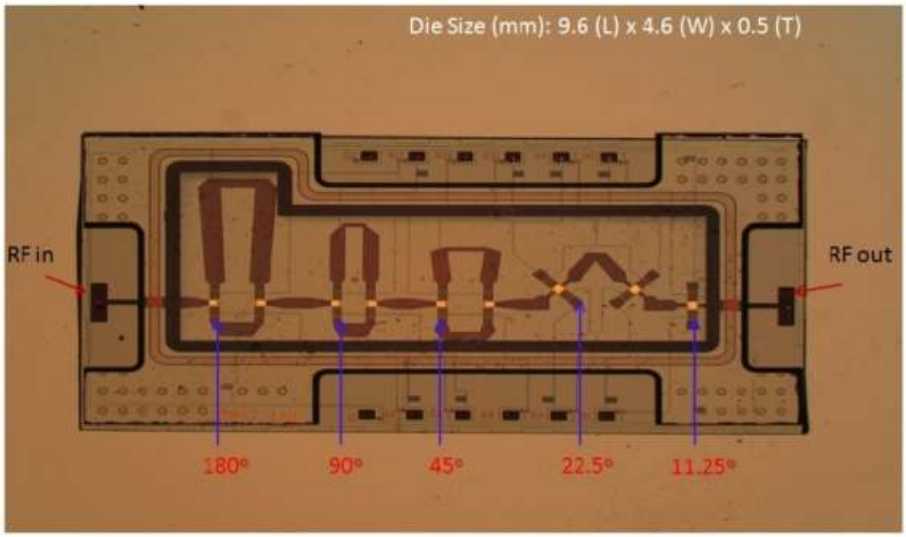


Fig. 8.6: Image of the fabricated microstrip version of phase shifter.

8.2 Test Jig Description

The die are realized on HR Silicon substrate and provided with 0-level Quartz cap. The MEMS die phase shifters have been placed in a recessed cavity realized in a multilayer RF substrate. Wire bonding interconnections have been used for both the DC and the RF signals. RF in and out have been designed to provide 50Ohms matching when using the RF end launch connectors provided together with the test jigs. DC connections are driven to the bottom part of the substrate through metalized vertical via holes. DC connectors are visible in Fig. 8.7 (a) and (b) along with the die. Every test jig is provided with an additional removable FR4 protection in light yellow as shown in Fig. 8.7(c), in order to further protect the MEMS die as well as the wire bonding. The FR4 is fixed by means of 4 lateral screws. The final view is shown in Fig. 8.7 (d)

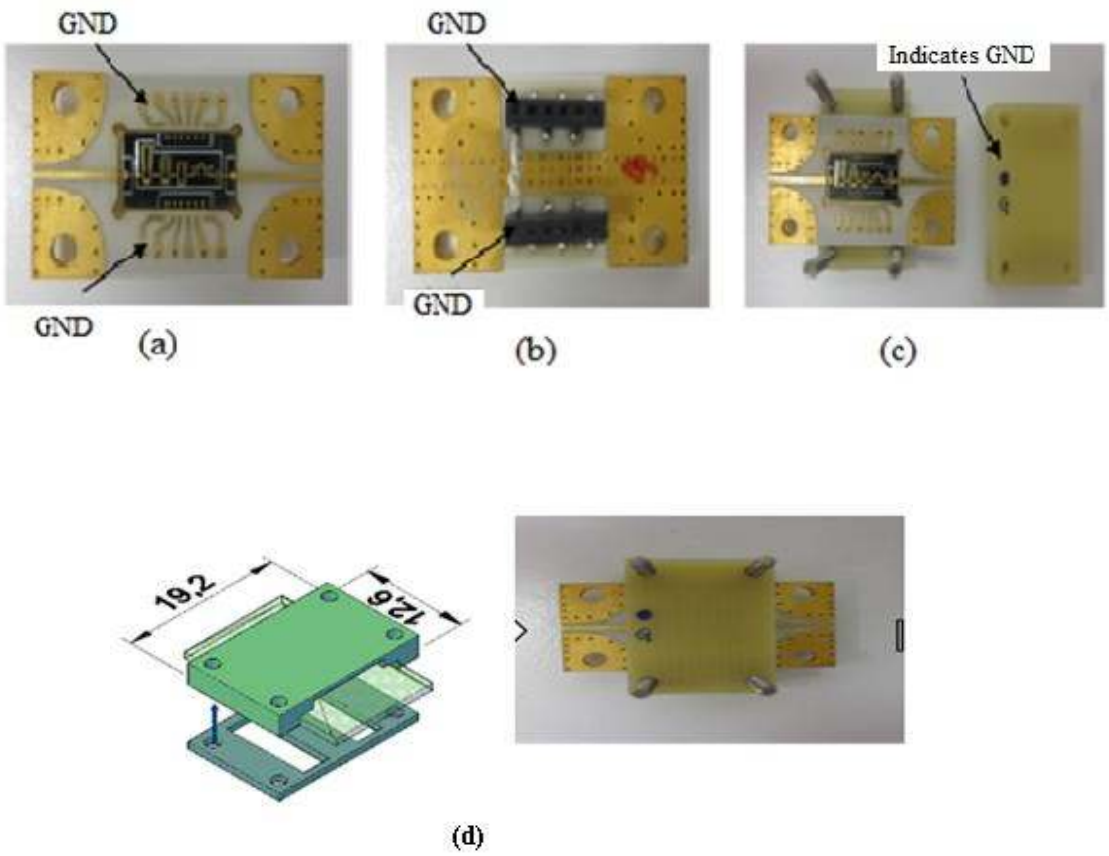


Fig.8.7: (a) and (b) dc interconnections along with die, (c) FR4 cap and (d) final view after assembly.

8.3 Control Circuitry Description

The control circuitry was developed to drive the phase shifter with the programmable microcontroller for logic combination having the high voltage driver. The Image of the control circuitry PCB hardware board and assembly of the die has been shown in the figure 8.8 (a). The control board has DIP socket shown in the enlarged view to accommodate the assembled the phase shifter on a test jig as indicated with a mark of G indication the ground. The 8.8 (b) depicts the integration of assembled substrate on to the hardware board for test purpose.

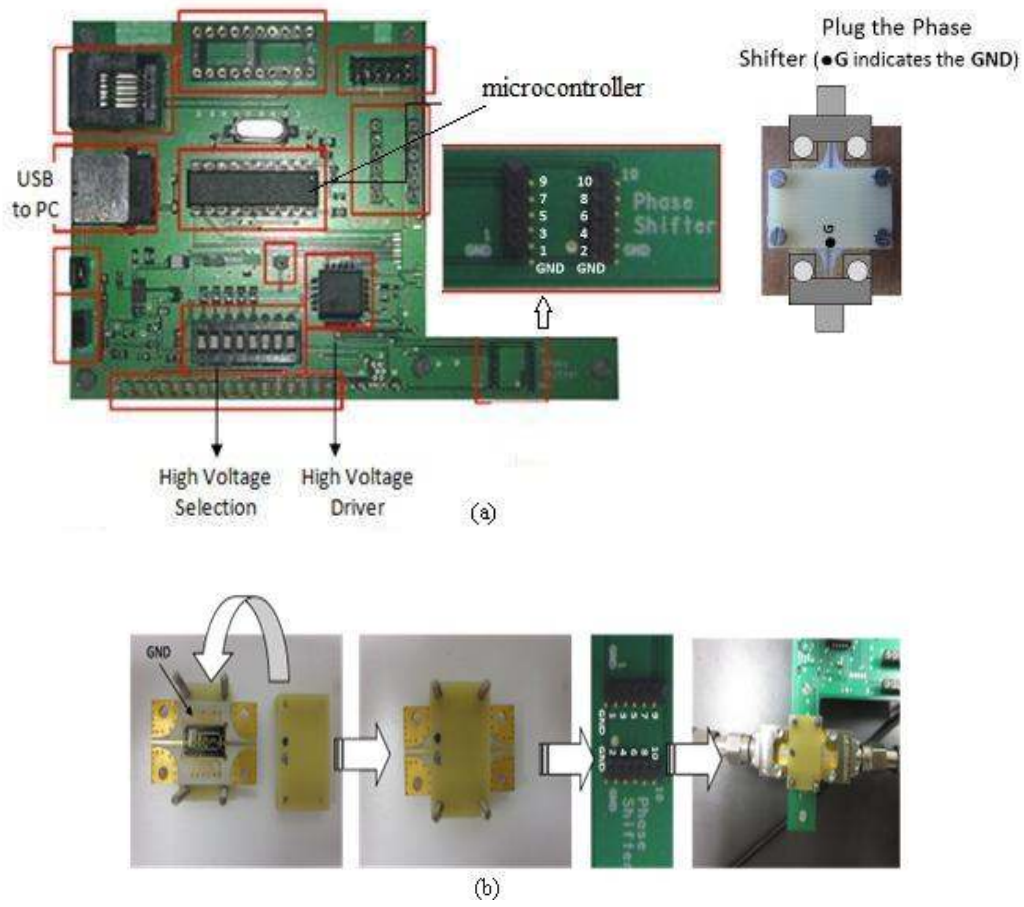


Fig. 8.8 :(a) Control board with its principal parts and (b) the mounting scheme of the assembled phase shifter on to the control board.

The DIP part of the control board has been highlighted in the Fig. 8.9 (a) and the following description shows the setting of voltages from 40V to 80V using the DIP switches. The Fig. 8.9(b) shows the test points on the board using a voltmeter to verify the actual voltage value setting before connecting it to the phase shifter jig.

i. High Voltage Output = 40V → Select the Pin Numbers: 1

ii. High Voltage Output = 50V → Select the Pin Numbers: 1 & 2

iii. High Voltage Output = 60V → Select the Pin Numbers: 1 & 2 & 3

iv. High Voltage Output = 70V → Select the Pin Numbers: 1 & 2 & 3 & 4

v. High Voltage Output = 80V → Select the Pin Numbers: 1 & 2 & 3 & 4 & 5

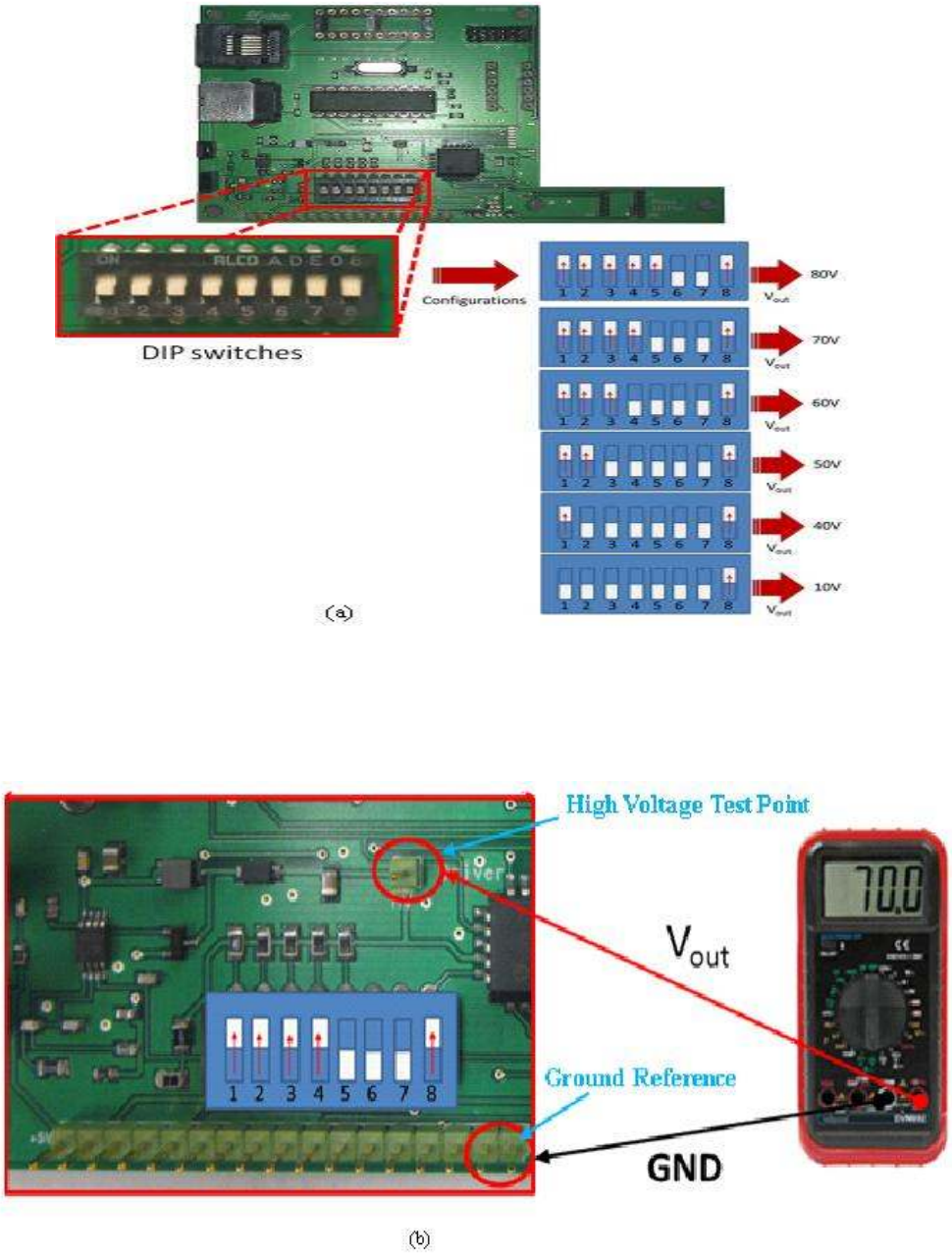


Fig. 8.9: (a) Switches combination and the V_{out} generated the DIP switch. (b) Zoom on the High Voltage Test Point to be used to verify the actual voltage value.

8.4 Graphical User Interface

The graphical user interface has been generated to carry the 32 states RF characterization by application of the logic control. The binary bit format will automatically

be generated once a particular phase shift value has been selected. The "Reset" button to reset all switches, i.e. deactivate all switches, corresponding to the "0000000000" binary word. This means all pins are connected to Ground. The graphic window is shown in Fig. 8.10.

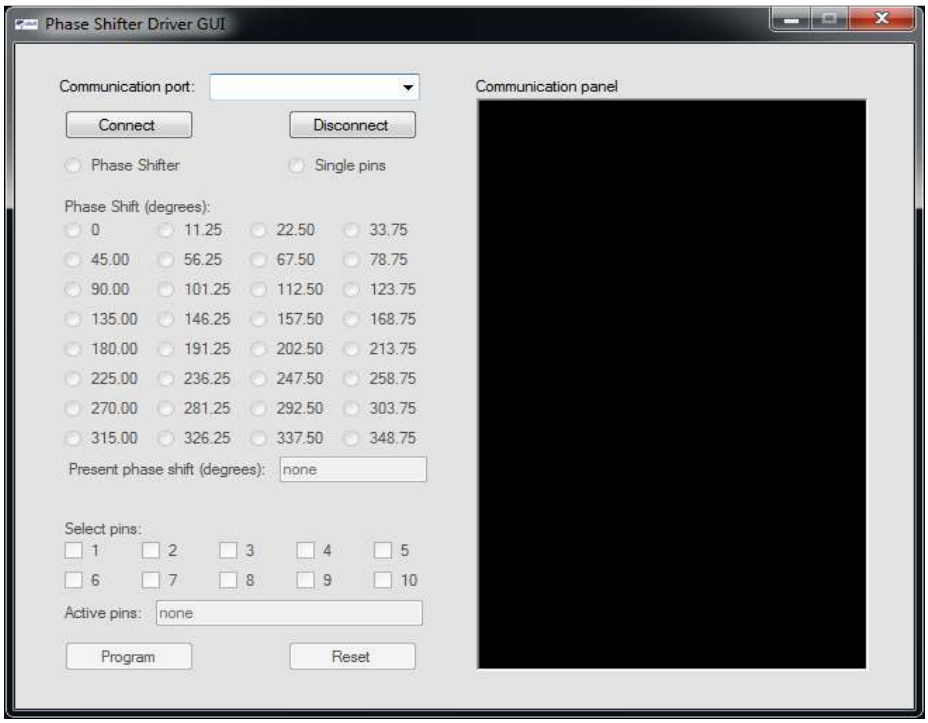


Fig. 8.10: The Graphic User Interface.

8.5 Hardware Setup

The hardware has been provided an USB port to connect for PC interface to control the 12 dc signals necessary to drive the 5-bit phase shifter for 32 states measurement. The interconnection test set up with Vector Network Analyzer (VNA), PC, Test jig and the control board are shown in the Fig. 8.11.

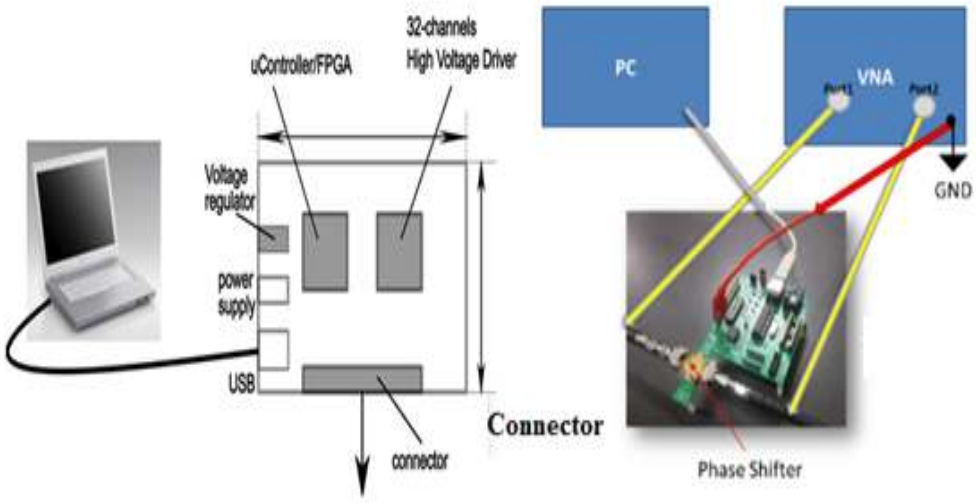


Fig. 8.11: Test set up configuration for microstrip phase shifter.

8.6 RF Characterization

The RF testing of the 5-bit microstrip phase shifter has been carried out as described in the above sections using different test support accessories like control board, test jig and GUI etc. The Image of the physical set up is shown in the Fig. 8.12.

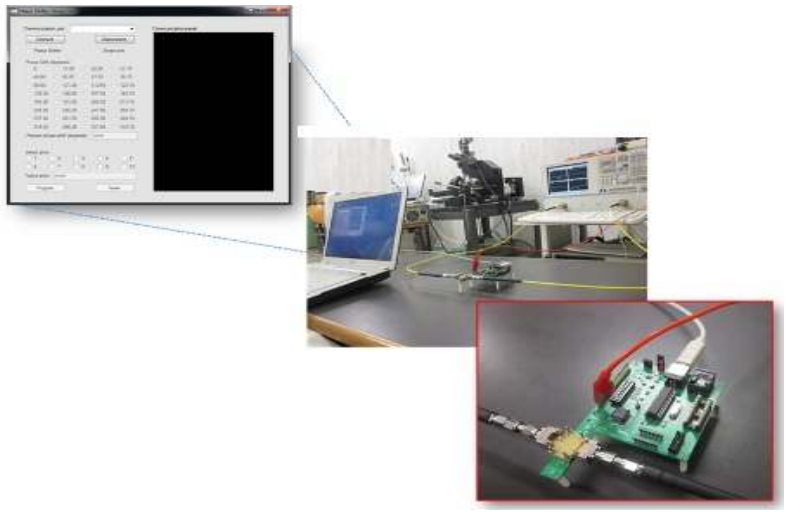


Fig. 8.12: Image of the physical set up of microstrip phase shifter.

The RF performance for the microstrip version is shown in the Fig.8.13 (a-d). The Measured return loss is better than 12.73dB and insertion loss better than 5.17dB for the 32 states in 16-18GHz frequency range. We found average insertion loss is 4.68dB (IL_{min} = 4.03dB, IL_{max}=5.17dB) and the phase shift error (rms) for the 32 states is 2.83degrees. This insertion loss includes the loss towards the RF connectors and the test jig which is of the order of 1.35dB. The effective loss of the microstrip version phase shifter is 3.33dB for 5-bit phase shifter over 32 states in the 16-18GHz frequency band.

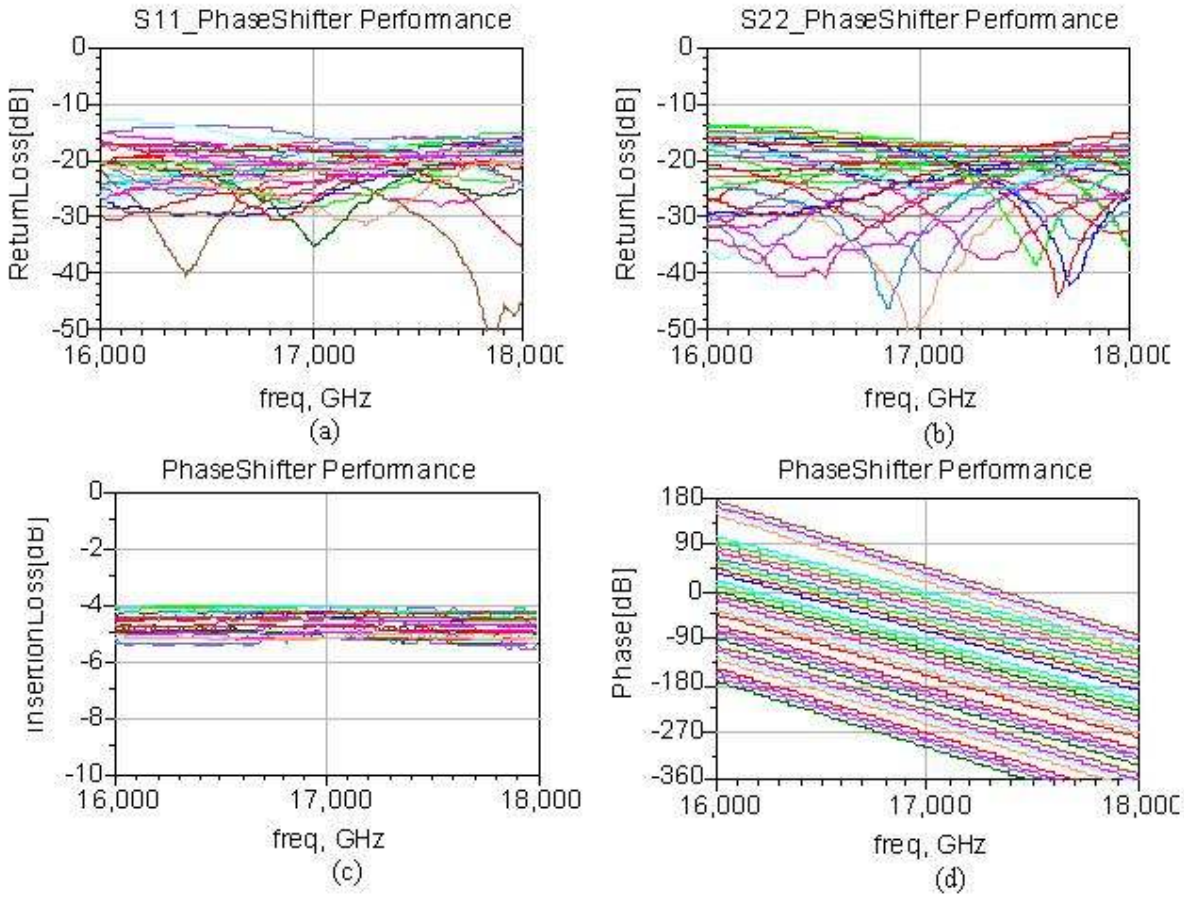


Fig. 8.13: Measured performances of the 5-bit MEMS phase shifter, (b, and c) Output/Input return loss, (d) Insertion loss, and (e) phase measured over 32 states.

Summary

In this chapter the test set up for microstrip version has been described. Various aspects of the assembly and interconnect optimizations have been discussed which covers the number of bonds and bond wire length. The jig characterization without phase shifter also has been done to ascertain the accuracy during measurement. A dedicated control circuit and GUI have been developed to perform the testing over the 32 states of the device. Finally RF results of the microstrip version of the 5-bit phase shifter are displayed which shows an unique achievement in this frequency band.

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CHAPTER 9

Conclusion and Future Work

9.1 Conclusion

5-bit MEMS phase shifter in Ku band is a strategic requirement for phased array systems in defense and aerospace applications. However there is paucity of systematic study of the 5-bit MEMS phase shifter in Ku band. Here in, we have taken up a systematic approach to develop a 5-bit Ku band phase shifter starting from the low actuation switch and phase shifter design and characterization.

We have successfully demonstrated the low potential capacitive shunt and ohmic switch with a novel design of split beam concept. Due to this unique design approach a low stress of the order of 380 MPa for the split beam configuration in comparison to that of 630 MPa in case of rectangular holes has been observed. Additionally, it has shown its ease in structural release due to large continuous area available for sacrificial release. These features have led to built-in reliability through design approach. The two design configurations for capacitive shunt configurations i.e. with single and double dc bias pad have been fabricated and RF results were compared for the critical parameters of insertion and return loss along with isolation. RF evaluation has shown an increase of 0.04 dB at 20GHz which is very negligible in case of single dc bias pad configuration. The single dc bias configuration can be conveniently implemented at subsystem level with other ICs and MMICs. Similarly ohmic switch has been successfully demonstrated with low actuation potential having very low stress in comparison to the rectangular holes approach commonly described in the literature.

The insertion loss 0.20dB and return loss 24.0dB have been achieved for capacitive shunt configuration. While for series switch insertion loss 0.18dB and return loss 21.0dB have been demonstrated. The above findings in RF results make these switches suitable for the reconfigurable circuits and phase shifter.

In the best of my knowledge this is first attempt to develop and implement a 5-bit MEMS based phase shifter in Ku band for the active phased array. The phase shifter design was carried out according to the process inputs from FBK foundry. Hybrid design approach of switched and loaded line configuration was adopted for the 5-bit design. The switched line was adopted for larger bits as it provides higher phase accuracy. The loaded line topology is preferable for smaller phase bits as these do not need higher loading and also it is less sensitive to variations of the contact resistance. Proposed design topology of phase shifter is tested with CPW configuration successfully.

Further microstrip version has also been developed to implement this in the T/R module of the active phased array. A RF test jig with dedicated control circuitry has been developed to test the microstrip configuration. The microstrip version has shown an average insertion loss of 4.68dB for the 5 bits at the jig level. This insertion loss includes the 1.35dB insertion loss due to test jig as it has been reported in the test jig evaluation. In true sense the microstrip version has shown average insertion loss as 3.33dB for the 5-bits in 16-18GHz frequency range.

In nutshell, contributions of this thesis are summarized below

a) Design, Simulation, Fabrication and Characterization of RF MEMS Switches

- Built in reliability concept through design of capacitive shunt and ohmic series Switches with a novel concept of the split beam.

- Achievement of low structural stress and high restoration force for stable operation. The structural stress lower by 35-40% and 25-30% in case of the capacitive shunt and series switch respectively with respect to standard holes configuration.
- The low actuation of 24.6V and 18.1V for the capacitive fixed-fixed membrane and ohmic series cantilever has been achieved respectively.
- Common process design for capacitive shunt and ohmic series switch.
- Successful fabrication of the switches on Quartz.
- RF parameters characterized using probe station has shown a very negligible degradation in the insertion loss in comparison to the simulated results. The lower insertion loss 0.24 dB (single bias pad), 0.20dB (double bias pad) for capacitive shunt switch and 0.18dB for ohmic series switch configurations have been achieved.

  The complete development makes these switches suitable for implementation into circuits like phase shifters etc.

b) Design and Development of 5-bit Ku band RF MEMS CPW and Microstrip Phase Shifter

- Design and simulation of the singular bits and integrated 5-bit phase shifter with CPW transition.
- The successful implementation of hybrid approach for 5-bit phase shifter as the best trade off among large phase shift, low loss and reduced space occupation i.e. 9x4.6 mm in the selected 16-18GHz frequency band.
- Fabrication of the phase shifter on high resistivity Si (>5 kΩ-cm).
- Development of test jig and control circuitry having high voltage drivers and microcontroller.
- Successful testing of the microstrip version phase shifter at the test jig level.

- On-wafer RF characterization of single bits and integrated 5-bit phase shifter meeting the desired RF results. The insertion loss of 3.33dB and phase error (rms) 2.83^{o} has been achieved for the 5-bits over 32 states in 16-18GHz.

  RF test results make them suitable for T/R module implementation in phase array applications.

9.2 FUTURE SCOPE OF WORK

- To optimize the 5-bit microstrip phase shifter design on GaAs with low actuation potential and extend the same for the 6-bit for higher resolution.
- Fabrication of the phase shifter on GaAs using Indian foundry.
- To develop a wafer level packaging with minimum insertion loss for environmental protection of the MEMS structure.
- Extension of RF MEMS phase shifter integration with the on chip high voltage drivers.
- Implementation of RF MEMS phase shifter as multifunction chips using MEMS and MMIC technologies.

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PUBLICATIONS

INTERNATIONAL JOURNAL ARTICLES

1. **Anesh K Sharma**, Ashu K Gautam, CG Balaji, Asudeb Dutta, SG Singh,"Ohmic RF MEMS Switch with Low Loss and Low Force on Quartz For Reconfigurable Circuits" *International Journal of Electrical and Electronics Engineering Research* ISSN 2250-155X, Vol. 3, Issue 1,45-54, Trans Stellar Publications, Jan- Mar 2013
2. **Anesh K Sharma**, Ashu K Gautam, CG Balaji, Asudeb Dutta, SG Singh, "Split Beam Low Force Low Loss Capacitive High Frequency MEMS Switch on Quartz For Reconfigurable Circuits" *International Journal of Electrical and Electronics Engineering Research* ISSN 2250-155X, Vol. 2, Issue 4,1-12, Trans Stellar Publications, Dec-2012.
3. **Anesh K Sharma**, Ashu K Gautam, CG Balaji, Asudeb Dutta, SG Singh, "Shunt RF MEMS Switch with Low Potential and Low Loss on Quartz for Reconfigurable Circuit Applications" *International Journal of Electronics and Communication Engineering & Technology* ISSN 0976-6464 (Print) ISSN 0976-6472 (Online), Volume 3, Issue2, , pp 497-510, July-September 2012.
4. **Anesh K Sharma**, Ashu K Gautam, DVK Sastry, S G Singh, "Design & Modeling of 6-bit low loss Ka band Distributed MEMS Phase Shifter on GaAs" *Advanced Materials Rese*arch Vols. 403-408,pp. 4179-4183, Trans Tech Publications, Switzerland, 2012
5. **Anesh K Sharma**, Ashu K Gautam, DVK Sastry, S G Singh, "Design & Simulation of low loss 5-bit Ku band Switched line MEMS Phase Shifter on GaAs" *Advanced Materials Rese*arch Vols. 403-408 pp. 5330-5334, Trans Tech Publications, Switzerland, 2012

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1) Anesh K Sharma, Ashu K Gautam, Paola Farinelli, Asudeb Dutta and S G Singh, "Ku band 5-bit MEMS Phase Shifter for Active Electronically Steerable Phased Array Applications" in ***Journal of Micromechanics and Microengineering,*** **IOP Publications.**

2) Anesh K Sharma, Ashu K Gautam, Asudeb Dutta and S G Singh, "Design and Fabrication of Low Phase Error Singular Phase Bits for MEMS Phase Shifter on HRS", ***International Journal of Electrical and Electronics Engineering Research, Trans Stellar Publications.***