HIGH PERFORMANCE CMOS WIDE-BAND RF FRONT-END WITH SUBTHRESHOLD OUT OF BAND SENSING

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Dedication

To my dear husband and beloved parents

Abstract

In future, the radar/satellite wireless communication devices must support multiple standards and should be designed in the form of system-on-chip (SoC) so that a significant reduction happen on cost, area, pins, and power etc. However, in such device, the design of a fully on-chip CMOS wideband receiver front-end that can process several radar/satellite signal simultaneously becomes a multifold complex problem. Further, the inherent high-power out-of-band (OB) blockers in radio spectrum will make the receiver more non-linear, even sometimes saturate the receiver. Therefore, the proper blocker rejection techniques need to be incorporated. The primary focus of this research work is the development of a CMOS high-performance low noise wideband receiver architecture with a subthreshold out of band sensing receiver. Further, the various reconfigurable mixer architectures are proposed for performance adaptability of a wideband receiver for incoming standards. Firstly, a high-performance low- noise bandwidth-enhanced fully differential receiver is proposed. The receiver composed of a composite transistor pair noise canceled low noise amplifier (LNA), multi-gate-transistor (MGTR) trans-conductor amplifier, and passive switching quad followed by Tow Thomas bi-quad second order filter based tarns-impedance amplifier. An inductive degenerative technique with low-VT CMOS architecture in LNA helps to improve the bandwidth and noise figure of the receiver. The full receiver system is designed in UMC 65nm CMOS technology and measured. The packaged LNA provides a power gain 12dB (including buffer) with a 3dB bandwidth of 0.3G – 3G, noise figure of 1.8 dB having a power consumption of 18.75mW with an active area of 1.2mm*1mm. The measured receiver shows 37dB gain at 5MHz IF frequency with 1.85dB noise figure and IIP3 of +6dBm, occupies 2mm*1.2mm area with 44.5mW of power consumption. Secondly, a 3GHz-5GHz auxiliary subthreshold receiver is proposed to estimate the out of blocker power. As a redundant block in the system, the cost and power minimization of the auxiliary receiver are achieved via subthreshold circuit design techniques and implementing the design in higher technology node (180nm CMOS). The packaged auxiliary receiver gives a voltage gain of 20dB gain, the noise figure of 8.9dB noise figure, IIP3 of -10dBm and 2G-5GHz bandwidth with 3.02mW power consumption. As per the knowledge, the measured results of proposed main-high-performance-receiver and auxiliary-subthreshold-receiver are best in state of art design. Finally, the various

reconfigurable mixers architectures are proposed to reconfigure the main-receiver performance according to the requirement of the selected communication standard. The down conversion mixers configurability are in the form of active/passive and Input (RF) and output (IF) bandwidth reconfigurability. All designs are simulated in 65nm CMOS technology. To validate the concept, the active/ passive reconfigurable mixer configuration is fabricated and measured. Measured result shows a conversion gain of 29.2 dB and 25.5 dB, noise figure of 7.7 dB and 10.2 dB, IIP3 of -11.9 dBm and 6.5 dBm in active and passive mode respectively. It consumes a power 9.24mW and 9.36mW in passive and active case with a bandwidth of 1 to 5.5 GHz and 0.5 to 5.1 GHz for active/passive case respectively.

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Chapter 1

Introduction

1.1 Introduction

Wireless communications have proliferated and penetrated into daily life as a result of decades of continuous advancements in communications and semiconductor technologies. With the introduction of new applications, services and the increasing demand for higher data rate comes the need for new frequency bands and new standards. A wide variety of applications, ranging from Global Positioning System (GPS), cellular communications, Wi-Fi Local Area Network, and short-range personal communications such as Bluetooth (BT), have been commercially deployed and continue to evolve. On the emerging horizon, mobile terminals no longer limit their usage to a single purpose, but serve to provide a multitude of access to heterogeneous networks over which rich service contents are delivered by concurrent or switchable operation of/among different link communications.

One critical issue for next generation wireless receiver for radar and military application is how to support multibands while not increasing the cost and power consumption. Multiple narrowband CMOS receiver front-ends with external RF filtering are well known approach in the past and the various efficient filter techniques were proposed to prevent large out-of-band signals corrupting the wanted signal. However, multiple RF front-end with filters make the system costly as well as bulky. So a feasible solution is the concept of the software-defined radio where

a single receiver can operate in different modes, each of which supports one or several bands and/or standards. To implement such a receiver, a wide band radio frequency (RF) building blocks, such as the Low Noise Amplifier (LNA), mixer etc., are required. Now, such multiband receiver LNA, picks up the strong in-band /out of band blockers signal from unintended uplink communications with the desired receiving signal. The amplitude of these blockers signals is usually much larger than the desired signal. If not appropriately corrected, they will affect the receiver response and block the healthy receiving of the intended signal. The impacts of blockers include desensitizing the receiver sensitivity, compressing amplifier gain and eventually driving circuits into saturation, increasing signal distortion and reciprocally mixing with LO phase noise, all of which deteriorates link performances such as receiver bit error rate.

Standalone radio mitigates the blocker issue by placing high-Q filters in front of the LNA to reject the unwanted signal energy. However, existing solutions rely on MEMS technology and needs to solve practical issues such as minimizing the extra fabrication cost and improving the yield. For at least three reasons, active filters have made little impact in super heterodyne receivers, where a bandpass filter with poles selects the desired channel at some intermediate frequency (IF). First, the power dissipation of an active bandpass filter rises proportionally to the center frequency and the required dynamic range. Second, it is increasingly difficult because of parasitic effects to accurately realize high poles at high center frequencies. Third, it is difficult to meet the specifications on distortion because the filter must handle signals and interferers which are amplified by the frontend. For these reasons, ceramic and surface acoustic wave (SAW) filters tuned to frequencies from 100's of kHz to 100's of MHz are used in vast numbers in production broadcast radio receivers and conventional cellular telephone handsets, but saw filter makes receiver narrowband. So for continuous wide band receiver a tunable RF filter suits better for dynamically reconfigurable blocker rejection. Our aim is to design low noise, wide band receiver for radar and satellite application with out of band blocker sensing and rejection at the input stage.

1.2 Aim and Motivation

(Complementary Metal Oxide Semiconductor)CMOS technologies with aggressive scaling improves area and power consumption with high enough f_T to accomodate most existing commerical applications under 10GHz. Compatibility with the digital part of the transceiver mandates the use of advanced (scaled down) CMOS process. With its ability of highest level of integration, low cost, and low power consumption, CMOS is a MUST for SOCs consumer electronic products.

Different communication standards exist currently where most of them are allocated in the spectrum from 400MHz to 6GHz . Traditionally, each standard requires separate RF front-end and digital resources for baseband processing. Presently, the existing designs are in form of single band specific L/S/C and the number of used chips also limited. This has given rise to a need for receivers that are compatible with as many standards and frequency bands as possible. Now a day, researcher in academic/industry is looking to integrate all L / S /C bands in the form of a single receiver in CMOS. So above approach is power hungry, costly and take more area. To exemplify this point, a multiband Radar/Satellite Receiver front-end can be designed

The noisy radio frequency (RF) environment demands a very stringent blocking requirement for most wireless applications. To address both inband/outband interference issues in broadband single receiver front-end (BSRFE), various blocker cancellation techniques are used to improve the dynamic range of receivers as (a) Notch filter [1]- [2], (b) SAW filter [3]- [4], (c) SAW less [5]- [6], (d) Coupled inductor in LNA [7], (e) N path filter [8], (f) Self-Interference Cancellation [9], (g) An Active Feedback Interference Cancellation Technique [10], (h) A Feedforward approach [11], (i) A Digital cancellation, etc. In digital cancellation, along with main receiver, an additional reference receiver is employed for capturing these blockers [12]. So, receiver must satisfy a certain blocking template defined at various blocker frequencies and levels. Here mostly out of band blockers have been considered.

Hence, in this dissertation, an out of band blocker sensing multipath scheme is depicted with a major focus in the design, analysis and realization of a high performance wideband receiver architecture. A subthreshold (ultra low power) receiver is designed for out of band sensing. In main path receiver, a high gain differential LNA with bandwidth enhanced noise figure

minimization technique and a passive mixer with linearity improved integrated baseband filter are proposed and verified in CMOS process. Further, a standalone re-configurable active/passive mixer stage is proposed and a comparison is drawn with previous passive one in simulation mode

1.3 Highlights of Research Investigations

- Comprehensive review of blocker rejection wireless receiver techniques for high performance receiver.
- Wide band and noise optimized LNA design techniques has been proposed.
- Detailed Analysis of impact of inductor on input matching, gain bandwidth and noise figure of LNA.
- Noise optimization by using LVT MOS and how it does'nt impact on input matching of LNA.
- High performance low noise, bandwidth extensive Main path receiver has been designed, simulated and fabricated in 65nm CMOS and verified by measurements.
- Subthreshold receiver or auxiliary path receiver for out of band sensing and rejection to achieve better linearity.
- Subthreshold LNA and active mixer is optimized for ultra low power and wide band.
- Reconfigurable Mixer in the form of Active/Passive, RF bandwidth, noise and power

1.4 Overview of Thesis Contribution

1.4.1 Blocker Rejection Wireless Receiver Techniques

A comprehensive review of out of band blocker rejection is presented. Blocker effects on various performance parameter like gain compression, DC offset, phase noise mixing, self mixing, sensitivity, IMD3/XMD of receiver, how it is impacting on various parameter of wireless front-end

receiver. Further Various blocker rejection techniques (onchip/offchip) of wideband receiver has been discussed to reject out of band blockers. Pros and cons of each technique is presented in brief. Further a brief introduction of wideband Radar/Satellite Receiver design challenges, proposed design concern on wireless receiver approach, identified blocker and their strength for desired bandwidth has been illustrated. A new approach is presented to reject out of band blocker by using a multipath scheme or auxiliary path receiver without effecting the performance of main path receiver.

1.4.2 High Performance Bandwidth Extension Low Noise Main Path Receiver

A wideband with low Noise RF front end receiver is extensively demanding in market for various application. The proposed receiver employs LNA, MGTR TCA, switching quad, biquad filtering. Wideband low noise amplifier is considered first main building block of receiver followed by mixer (active/passive). Wide band receiver performance parameter like input matching, noise, gain are mainly limited by LNA. The impedance matching of LNA is considered to be more essential for wide band design to achieve wide band gain and noise flatness in lower technology node designs. In general, passive components (in particularly inductors) realized in present day CMOS technologies, exhibit considerable resistive losses (finite Q-factor) are used to enhance bandwidth. To achieve below 1.7dB noise figure is still challenging in CMOS technology and in this context NMOS/PMOS cross coupled transistor pair LNA technique is chosen to improve performance like gain BW and noise figure. This approach also cancel the noise generated by input transistor, hence lowers the noise figure. Degenerative inductor is introduced at the source of mosfet to achieve wide band input matching and gain flatness at higher frequencies. Further provide better headroom voltage headroom in cascode topology RVTMOS is replaced by LVTMOS. After replacing RVTMOS with LVTMOS to provide equivalent gm (maintaining gain and input matching) aspect ratio of LVTMOS is reduced. Thus it is concluded that thermal noise will decrease by using LVTMOS as width of the MOS decreases. By decreasing width with maintaining same gm achieved noise figure of LNA with LVT MOS is 1.2dB. Thus resistive feedback LNA noise can be further reduced by using LVTMOS. Further a passive mixer (including

TCA, switches and TIA) is incorporated. Linearity cancellation technique (MGTR TCA) is incorporated in TCA to achieve high linearity. Tow Thomas biquad filtering is applied to relax the linearity requirement of the following stage. Further all blocks are integrated in 65nm CMOS technology, taped out, fabricated. This concept is validated through a circuit simulations and real time measurements.

1.4.3 Auxiliary Path Ultra low power Out of Band Sensing Subthreshold Receiver

In recent days, the subthreshold bias technique is being preferred for realizing ultra low power receivers by exploiting the advantage of high g_m/I_D in this region. However, circuits designed in subthreshold region face design ambiguity due to the rise in parasitic capacitances and reduction of transit frequency (f_T). To overcome these issues, appropriate circuit techniques using passive components need to be incorporated. To design, wide band receiver with ultra low power is a major challenge. In this receiver, a fully integrated receiver frontend which is composed of a low-noise amplifier and a down conversion mixer is designed for multiband applications. The DC power reduction is achieved by driving the MOS in subthreshold region. However, achieving good input matching in presence of larger devices is a challenging task. Moreover, the increased thermal noise of MOS transistors in weak inversion region imposes the need of noise cancellation circuitry which increases the power consumption. Hence, conventional topologies such as common gate, resistive feedback, distributed amplifier and Complementary MOS circuit cannot be applied as it is, for realizing a low power wideband LNA in subthreshold LNA. To implement a low power ultra wideband LNA in subthreshold region, the conventional common gate topology is modified to provide wideband input matching and a current reuse noise cancelling technique is introduced to improve noise performance. Further to implement a low power ultra wideband down conversion mixer in subthreshold region, the conventional gilbert cell topology is modified. A RC degeneration is used to formulated wide band mixer. By introducing capacitive degeneration a zero has introduced in transfer function to increase gain bandwidth. and resistive degeration is compensated by cross coupling the input RF signal. A wideband RF front end receiver operating from 2G - 5GHz is designed in a 180nm RFCMOS technology, for out

of band blocker sensing. This concept is validated through circuit simulations and real time measurements.

1.4.4 Reconfigurable Down Conversion Mixer

To get a cost effective solution, a re-configurable single radio (that can configure to multi-mode as need basis) would be the best choice. To make the radio reconfigurable researchers introduce the RF transceiver front-end with reconfigurable LNA, PA, PLL, mixer, and filter etc. Among them, our emphasis is to design a Mixer that can provide reconfigurability on the performances like gain, linearity, noise figure and RF and IF bandwidth selection. Most of proposed reconfigurable mixer have shown gain variability and bandwidth tuning through current variation, load tuning etc.

1.4.4.1 Reconfigurable Active/Passive Down conversion mixer for wideband Receiver

Wideband (WB) reconfigurable down-conversion mixer for multi-standard wireless receivers is designed. The proposed mixer is re-configurable between active mixer and passive mixer modes. Reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. The proposed circuit is designed in UMC 65nm RFCMOS technology with 1.2V supply voltage. This concept is validated through circuit simulations and real time measurements. Hence this circuit will be much helpful in multi-standard receiver design in IoT perspective.

1.4.4.2 A Low/High Band Parallel path TCA with configurable (Active/Passive) Down Conversion Mixer

Down conversion mixer described in avove section has configurability between active and passive modes with gain and noise tunability but there is no configurability in RF bandwidth. To Reconfigure RF bandwidth, a down conversion mixer for a multistandard wireless receiver, with

adapted reconfigurability in the form of RF bandwidth, active/passive and IF bandwidth is proposed. In the proposed architecture RF bandwidth reconfigurability is reconfigured between low band (LB) RF frequency and high band (HB) RF frequency mixer modes. LB/HB reconfigurability is made through power switching the transconductance amplifier. Active/Passive reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. The proposed circuit is designed in the UMC 65nm RFCMOS technology with 1.2V supply voltage

1.4.4.3 Reconfigurable High/Low band Passive Down Conversion mixer for wide band Receiver

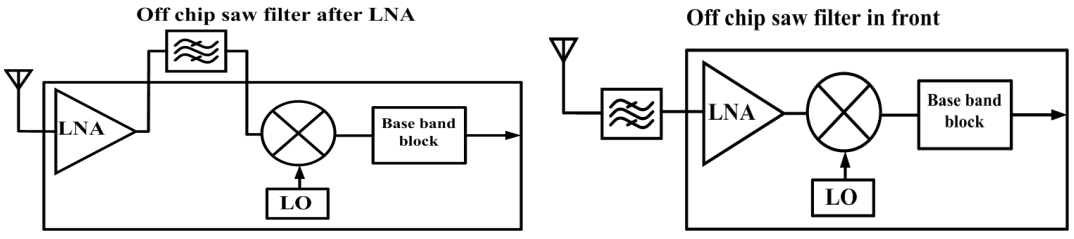
In above section RF configurability is done by power switching HB/LB transconductance amplifier. Further to reduce the area of the chip down conversion mixer is designed with RF bandwidth reconfigurability in single circuitry by using switches. This reconfigurability is in the form of RF bandwidth, power consumption. In the proposed architecture RF bandwidth reconfigurability is reconfigured between low band(LB) RF frequency and high band (HB) RF frequency mixer modes. LB / HB reconfigurability is made through switching the transconductance amplifier between these two modes. So power can be saved while operating in desired mode. The proposed circuit is designed in UMC 65nm RFCMOS technology with 1.2V supply voltage. Full inductorless can operate over a wide frequency range.

Chapter 2

Blocker Rejection Wireless Receiver Techniques

2.1 Introduction

Any wireless receiver, receives signal transmitted by antenna, A wireless receiver front-end down shifts the frequency and demodulates the signal to retrieve the transmitted data. Receiver main blocks are LNA and mixer, shown in Fig. 2.1 which performs band selection, amplification and frequency down conversion. Whereas baseband section does channel selection, additional amplification (if required), demodulation and retrieval of data.



(a) Off chip saw filter after LNA (b) Off chip saw filter in front

Figure 2.1: Saw filter based receiver.

The most important specifications of a RF receiver (saw or saw-less) is its sensitivity and

selectivity. Receiver sensitivity is the weakest signal level, it can detect with acceptable signal-to-noise ratio (SNR). Whereas selectivity is a measure of immunity to interferers and blockers close to its working frequency. These parameter can degrade the receiver performance such as noise figure and linearity. Saw filter based design are very famous for narrow band receiver as shown in Fig. 2.1(a) and Fig. 2.1(b) to remove out of band blocker (to achieve better linearity). In this chapter various metrics of blocker has been discussed in detail, and particularly their impact on receiver performance. Further various techniques have been explored to reject out of band blocker.

2.2 Effect of Blocker on Wideband Receiver

Most of the communication standards are allocated from 400MHz - 6GHz as shown in Fig. 2.2. Traditionally any receiver, receives all the band simultaneously from antenna, so there is a need to reject undesired band at the input of receiver otherwise receiver performance will reduce.

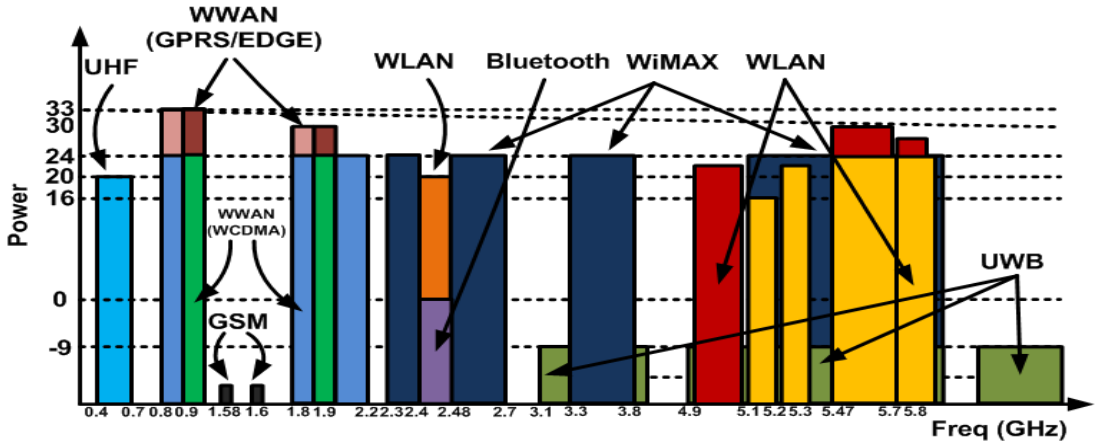


Figure 2.2: Crowded radio spectrum with multiple standards

The noisy radio frequency (RF) environment demands a very stringent blocking requirement for most multiband applications. Generally, the blocker may affect the receiver in two ways, 1) a large out-of-band blocker can saturate the receiver frontend, and hence by reducing the receiver gain, elevate the noise contribution of the following baseband blocks. 2) an in-band blocker may desensitize the receiver due to reciprocal or spurious mixing, or through inter-modulation. While

the in-band blockers are typically removed by adjusting the local oscillator (LO) phase noise and linearity of the receive path, and ultimately through baseband filtering. The large out-of-band blockers may only be eliminated through front-end filtering otherwise it effects serious issues on receiver shown in Fig 2.3. Thus removing this type of interference is considered as a crucial issue in designing RF transceivers.

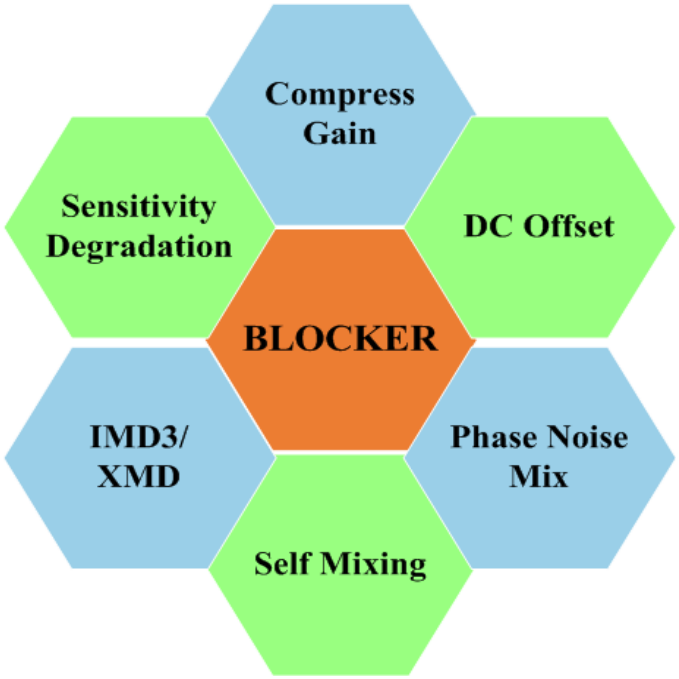


Figure 2.3: Effects due to blocker and transmitter leakage blocker on wideband receivers

2.2.1 Blocker Impact on Various Parameter

Blocker and Tx leakage may affect the receiver by following ways shown in Fig. 2.4 in the form of [13]. The problem of gain compression is demonstrated in Fig. 2.5. A conventional wide band design has no selectivity and amplifies both the wanted signal and any blockers present Fig. 2.5. Given the voltage amplification required to achieve a competitive noise figure and the low supply voltages used in modern CMOS processes, a 0dBm blocker will cause the LNA to clip. This will increase noise and distortion in the receiver. Since the desired signal is weak, the low-noise amplifier (LNA) gain must be kept high.

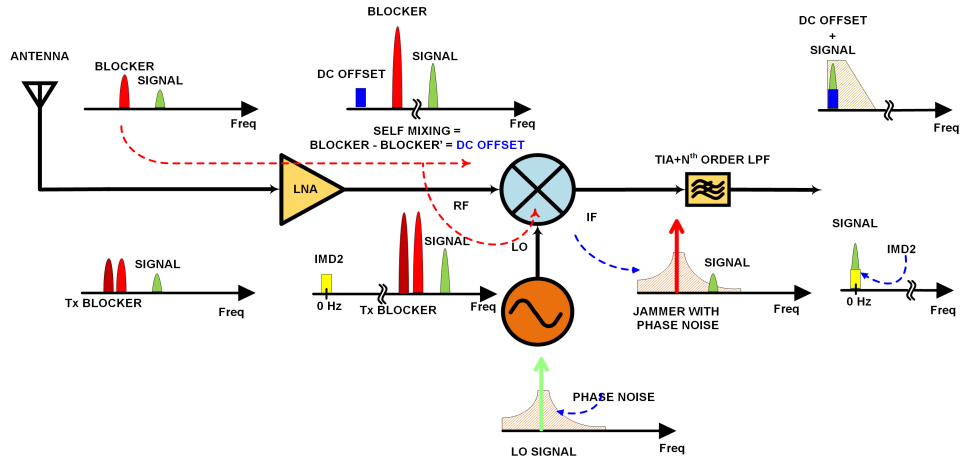


Figure 2.4: Issues due to blocker on wideband receivers.

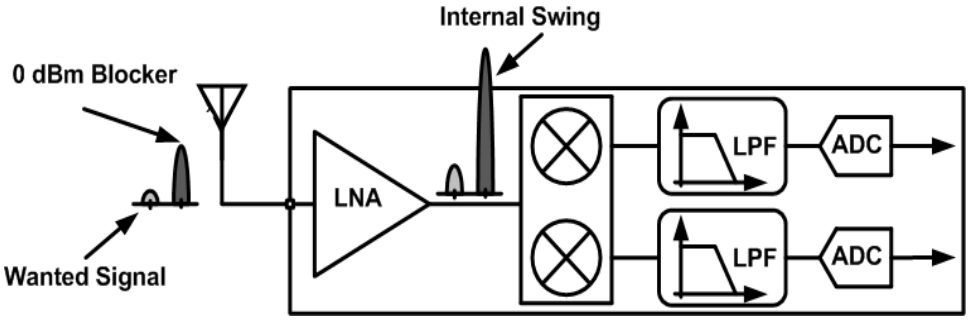


Figure 2.5: Gain Compression due to blocker

Similarly once blocker amplified by LNA, may find a path to the LO input port of the mixer, thus producing self mixing shown in Fig 2.4, which is a DC component at the mixer output and aggravates sensitivity as well. In addition, if the blocker has high phase noise, which also contributes to the overall noise floor level. If blocker has low phase noise and Rx LO has finite phase noise that mixes with blocker, and creates reciprocal mixing at the mixer output, degrades sensitivity also. If the blocker is near to receiver signal, blocker and transmitter leakage will cause 3^{rd} order intermodulation (IMD3) and cross modulation(XMD) simultaneously due to LNA nonlinearity. Both IMD3 and XMD are near to receiver signal, resulting in sensitivity degradation. Besides, if the blocker is near to transmitter signal in spectrum, LNA nonlinearity also causes IMD2, which is like DC offset, and will aggravate sensitivity. Blocker affect has summarized in Table 2.1 and thus the blocker must be filtered prior to reaching the amplifier

	With blocker	With blocker and Tx leakage
Gain Reduction	yes	yes
DC Offset	yes	yes
Self Mixing	yes	yes
Phase Noise	yes	yes
Reciprocal mixing	yes	yes
IMD3		yes
XMD		yes
IMD2		yes

Table 2.1: Blocker effect on receiver.

output. On the other hand, due to the modest quality factor (Q) of on-chip inductors, it is not practical to integrate such a sharp filter on-chip. For these reasons, all the existing receivers inevitably use an external surface acoustic filter.

2.3 Wideband Radar/Satellite Receiver design Perspective

Today, L/S band (1-2GHz, 2-2.7GHz) radio are widely spread in various defense, military and satellite applications. Presently, the existing designs are form of single band specific to one of L/S band and the number of used chips also limited. Although CMOS technology is cost effective (mass scale perspective), less area and power consumption but they commercially accepts more than 6 numbers of wafer. So these radios is designed in costly III-V technology as these foundry commercially accepts single wafer solution. Now a day, researcher in academic/industry is looking to integrate all L [14] [15] [16] [17]/S [18] [19] [20] [21] [22]/C [23] [24] [25] bands in the form of a single receiver in CMOS and also how to implement a highly integrated RF front-end that can operate at low power consumption without compromising the performance. To exemplify this point, a multiband Radar/Satellite Receiver front-end can be designed in the form of in Fig. 2.6 [26] and Fig. 2.7 [27].

But there are several disadvantages of using saw filter in wide band receiver.

1. It increases the cost, especially in multimode and multiband applications where several of these filters are needed.

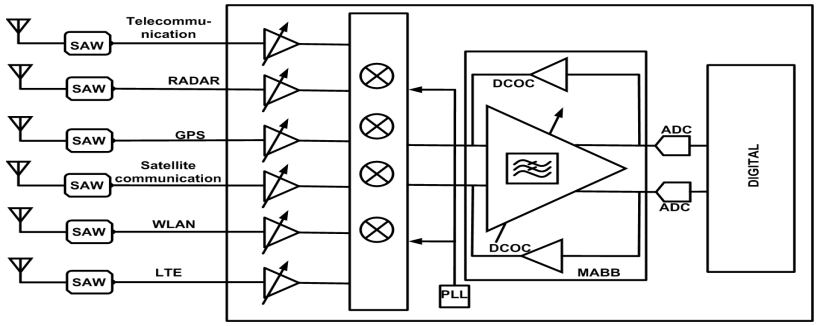


Figure 2.6: Multi-band receiver each path saw in front

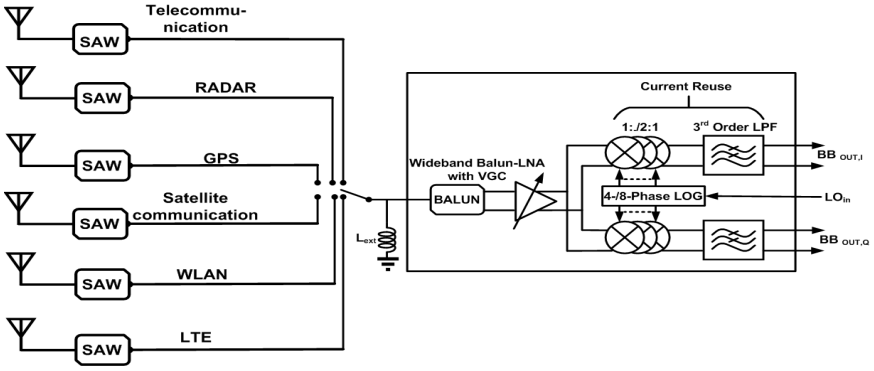


Figure 2.7: Wide band receiver with configurable saw in front.

2. The insertion loss of the SAW filter, typically as high as 2–3 dB, directly degrades the receiver sensitivity.

3. It removes the flexibility of sharing the LNAs in multimode or multiband applications, and particularly in software-defined radios.

Therefore, it is highly desirable to eliminate external saw filters. But it is important to remove blocker at input otherwise it can degrade receiver performance, so on-chip blocker removal techniques like feed-forward and feed-backward approach need to be investigated into these designed.

2.3.1 On Chip Blocker Removal Techniques for Wide Band Receiver

The problem of interference removal has been studied extensively in the past in various contexts, including background noise reduction in acoustic systems. These techniques employ mainly

out of band rejection by having on-chip filtering. To address outband interference issues in

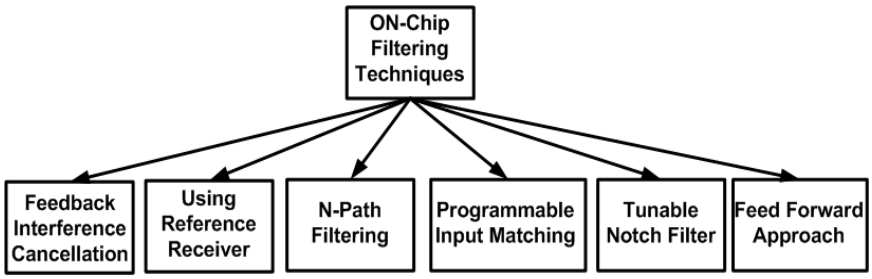


Figure 2.8: Blocker removal techniques

broadband single receiver front-end (BSRFE), various on-chip blocker cancellation techniques has been proposed, as shwon in Fig. 2.8 are used to improving the dynamic range of receivers as (a) Passive on-chip filtering [28],(b) Notch filter [1]- [2], (c) Coupled inductor in LNA [7], (d) N path filter [8], (e) Programmable filter [29], (f) Self-Interference Cancellation [9] (g) An Active Feedback Interference Cancellation Technique [10],(h) A Feedforward approach [11], (i) A Digital cancellation by using reference receiver etc. [12]. But passive filters are hard to tune, which makes design non tunable and narrow band, so feedforward and feedbackward design came into picture.

2.3.1.1 Feedforward

One way of reducing the out-of band blocker is through feed-forward injection shown in Fig. 2.9, where a replica of the blocker is subtracted at the LNA output. In order not to reject the desired signal as well, a notch filter in the feed-forward path is needed to distinguish the signal from the blocker. The notch filter should be centered at the desired RF bandwidth, rejecting the wanted signal, but must be sharp enough to pass the blocker, But feedforward techniques limited to narrow band design and are used for attenuating close-in interferers at RF is described [12]- [30]

2.3.1.2 Feedback Interference Cancellation

In this technique RF bandpass filtering using feedback interference cancellation are made. The concept of active feedback interference cancellation is shown in Fig. 2.10 [31]. The incoming wanted and blocker signal are amplified by an LNA with LC tank load. The output signal

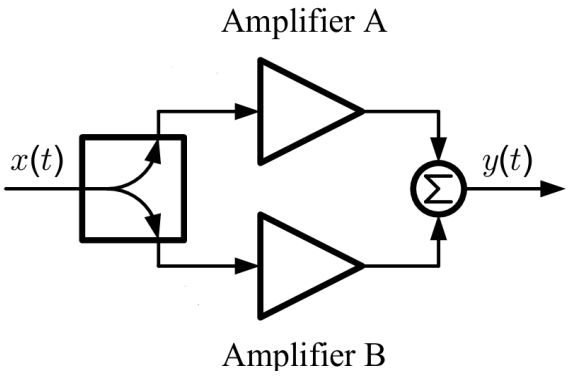


Figure 2.9: Feedforward linearization technique

is fed into the active cancellation filter core and downconverted to baseband by the receiver local oscillator signal. In order to boost the open loop gain, baseband amplifiers might be necessary. The wanted signal is eliminated by highpass filtering, a blocker replica is upconverted to RF and subsequently subtracted from the incoming blocker signal at the output of the LNA transconductor stage thus resulting in a partial cancellation of the blocker signal. In that sense, the interference cancellation loop acts as a control loop which suppresses the blocker by the open loop gain.

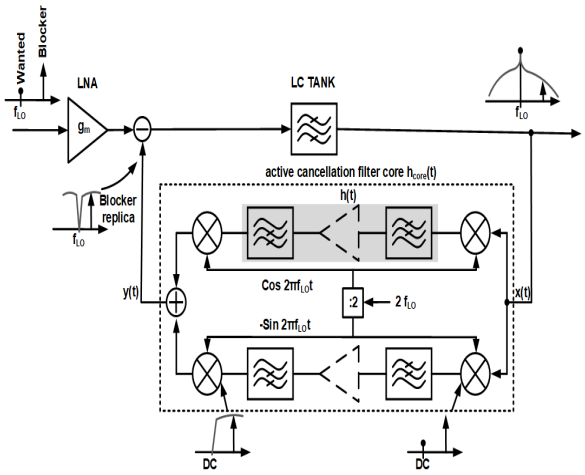


Figure 2.10: Block diagram of feedback cancellation mechanism.

Similar to feedforward, feedback techniques also has some constraint, note that the mixers act as up and downconverters simultaneously in this technique. Thus, the downconversion mixer

does not only generate a baseband component but also an RF signal at twice the LO frequency. All issues are discussed in detail [31]. Thus, it is difficult to design if IF bandwidth is more.

Our aim to design a receiver having bandwidth (0.3G- 3G) for radar and satellite application, which covers L band, S band. Due to many application like aircraft radar, TV broadcasting, mobile and cell phones, Wi-Fi, bluetooth, Taxi wireless, wireless LAN, cordless phone. ameteur wireless, private wireless, microwave, satellite communication etc it (multiband receiver) demands strong out of band blocker rejection technique. Our aim to reject out-band interferer signals at the input stage in such a way that there will not be much extra increase in power consumption and no effect on noise figure and other parameters. For these kind of wide band receiver a simplest multipath (auxiliary) receiver approach has proposed for multiband design. In main path receiver, a high gain differential LNA with bandwidth enhanced noise figure minimization technique and a passive mixer with linearity improved integrated baseband filter are proposed, and verified in CMOS process. For out of band sensing a auxiliary receiver (subthreshold) receiver is designed and verified in CMOS process. Specification of receiver for radar and military application is given in Table 2.2.

Standard	frequency bands	Gain (dB)	NF (dB)	IIP3 (dBm)
L1	1575.42MHz	51dB	3	-5
L2	1227.6MHz	53dB	4	-9
L3	1176.45MHz	55dB	3	-10
S	2750MHz	27	3.88	-15
S	27750MHz	27.29	4.07	-12
S	2800MHz	26.49	4.31	-11
S	2825MHz	26.35	4.37	-16
S	2850MHz	25.71	4.56	-13
GSM	0.8-1.9GHz	30	max 9dB	-16
3GPP-LTE	0.8-2.6GHz	30	3dB	-6
WiMAX	2.4-3.5GHz	30	3.5	-11
DVB-H	0.47-1.7GHz	30	3	-8
WLAN	2.4-5GHz	30	5	-8

Table 2.2: Receiver specification for radar and satellite Application

2.4 Proposed Design Concern on Wireless Receiver Approach

2.4.1 Identified Blockers and Strength

Indentified interfenrence in between frequency range 2-5GHz, is Wi-Fi. There are basically five frequency bands used for Wi-Fi technology, 2.4GHz, 3.65GHz, 4.9GHz, 5GHz, 5.9GHz. So 3 - 5 GHz ultra wide band identified interference are 3.65GHz, 4.9GHz and 5GHz shown in Fig. 2.11. Most wireless products use the following Wi-Fi spectrums: 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac.

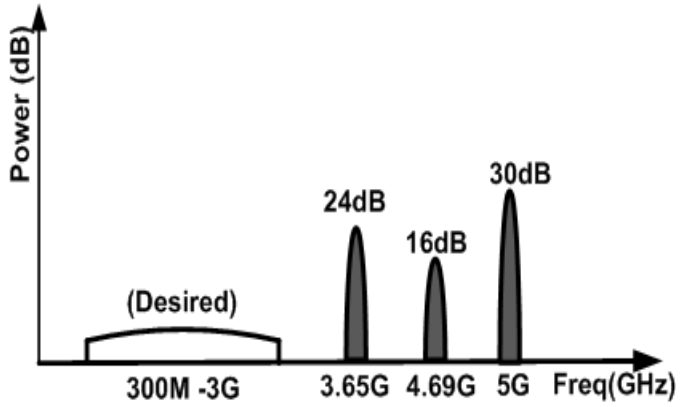


Figure 2.11: Identified out of band blocker

2.4.2 Proposed Design Approach

High Performance receiver (0.3G-3G) with subthreshold out of band sensing Receiver shown in Fig. 2.12. Subthreshold receiver is designed in such a way that it doesn't consume much power, senses out of band signal (3-5) GHZ and tuned the notch filters accordingly to reject out of band blocker at input. Two tunable notch filter centered at 4GHz is used and can be tuned from 3-4GHz or 4-5GHz constant distance (left and right from 4GHz).

An architecture of proposed approach for interference cancellation in receivers is shown in Fig. 2.12. The receiver consists of two paths. The front-end high performance receiver having

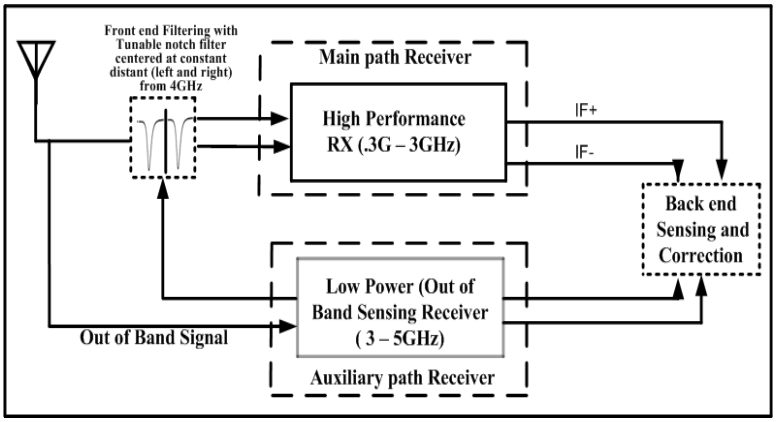


Figure 2.12: High Performance CMOS Wide-Band RF Front-End With Subthrehold Out of Band Sensing

differential LNA and down-conversion mixers form the main path is assumed to employ direct down-conversion. An auxiliary path receiver includes subthreshold LNA down-conversion mixers connected to the input of the main path which senses the out of band interferences and tune the notch filters located at fixed frequency 4GHz and tunes left and right from 4GHz according to the available RF band. The RF power incident on the antenna is assumed to consist of a desired signal and interferers. In the auxiliary path, the receiver will tune the notch filter for out of band frequency (3GHz - 5GHz) so that main receiver doesn't get saturate with interferers. If any out of band frequency interferer is present auxiliary path receiver with tune the notch filter to reject or attenuate the interferer. Tunable notch filters are used to attenuate interferers. If any blocker left, is down-converted to baseband with a local oscillator frequency (LO) are corrected by using back end correction. Back end sensing and correction can be done by using digital cancellation mechanism as used in [12].

2.5 Summary

This chapter has explored the fundamentals of RF receivers and its key performance parameters in brief. A review of effect of blocker and transmitter leakage on receiver has been presented. Various blocker rejection techniques has been studied. Among different techniques, Mutiband with each path saw in not good approach, as it makes receiver narrow band. Further feedward

and feedback techniques came into picture but these techniques are either for RF close-in band interferences or very complicated to design. Among this these techniques are for narrow band design. After looking all techniques multipath receiver seems to be a good one, so for radar and satellite application, a low noise wideband receiver with subthreshold out of band sensing solution has approached.

Chapter 3

High Performance Low Noise Main Path Receiver

3.1 Introduction

In a receiver, the low-noise amplifier (LNA) serves as the first amplification block along the receiving path. As it is one of the most critical building blocks of the receiver, since its performance greatly affects both the sensitivity and selectivity of the system. In this chapter, we will analyze the basic properties of a CMOS LNA. Starting with a discussion of receiver specification in section 3.2. Finally, will present a review of input matching and noise cancellation techniques of low-noise amplifier topologies, followed by analyses of input matching, noise, gain, bandwidth, implementation and measurement result.

In the next section, we will discuss the architecture of the demodulator, The mixer is one the most important nonlinear blocks in all wireless receivers. The primary function of a mixer is to perform frequency translation of the signal between the carrier frequency and baseband. The mixer's performance strongly affects the overall performance of the receiver, and it is a major nonlinear component in the receiver front-end. Finally we will discuss the architecture of the demodulator, followed by the circuit details of the various blocks, then implementation,

measurement results of complete receiver and conclusions.

A review of performance of recently reported low noise wide band receiver is listed in Table 3.1. For wideband operation choice of LNA and mixer topologies plays very important role. Various paper of LNA and mixer paper has been reviewed and listed in below sections. Low noise composite transistor pair LNA is better topology for desired bandwidth (WB) and further inductive degeneration is used for bandwidth extension. Similarly for down conversion mixer, passive mixer is the best one for low noise, power and direct conversion. In below sections, wideband input matching and noise cancellation topologies of LNA and downconversion mixer operation are discussed in detail.

Table 3.1: Review of recent wideband receiver

Ref.	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)	Area (um^2)
[13]	0.3-2.9	58	<-10	1.9-2.1	+12	1.3	49.4-99.8	40	1100*1100
[32]	0.05-2.4	80	<-10	5.5	27	1.2/2.5	60	65	2000*2000
[29]	0.4-4	36	<-15	3.5 7	2.5	1.2	38.4-55.2	65	
[33]	0.6-3	42-28	<-8	3	-14	1.2	30	130	1500*1000

3.2 Wide Band Receiver Design Specification

3.2.1 Sensitivity

Sensitivity of receiver is normally taken as the minimum input signal (S_{min}) required to produce a specified output signal having a specified signal-to-noise (S/N) ratio and is defined as the minimum signal-to-noise ratio times the mean noise power given by (3.1). Sensitivity is expressed in terms of dBm (decibels relative to one milliwatt) power level along with reference impedance (usually 50Ω) at the matched input condition.

$$S_{min}(dBm) = -174 + 10 * Log_{10}(BW) + NF_{rx} + SNR_{min} \tag{3.1}$$

where BW is signal bandwidth, NF_{rx} is total receiver noise figure, and SNR_{min} is minimum required signal-to-noise ratio. If $T_0 = 290K$.

3.2.2 Noise Figure

Sensitivity and system noise figure are two closely related parameters for a wireless receiver. Noise Figure (NF) is the parameter which impacts the achievable sensitivity of a receiver. The relation between sensitivity and noise figure is given in (3.1). Noise factor F is defined as the ratio of input signal-to-noise SNR_{IN} to output signal-to-noise SNR_{OUT}. Noise figure NF is actually the noise factor in dB, i.e.

$$NF = 10 * \log(F) = 10 * SNR_{IN}/SNR_{OUT} \tag{3.2}$$

3.2.3 Selectivity

Selectivity is the maximum signal level that a receiver can demodulate, and decode the information without an error in the presence of much stronger interferers (in-band/out-of-band). Selectivity of any receiver depends on filter sharpness of both RF band select filter and IF channel select filter, the dynamic range and circuit non-linearity.

3.2.4 Linearity

In practical scenario no system is purely linear. which always distorts the output signal when the input signal level is above some threshold value. The inherent non-linear transfer characteristics of active devices (like BJT, MOS) impose this threshold. A practical non-linear system may be represented as

$$y_t = a_0 + a_1 * x_t + a_2 * {x_t}^2 + a_3 * {x_t}^3 + ... \tag{3.3}$$

However, we are interested in achieving a linear system by making all coefficients other than first order gain (a_1) zero. Effects of non-linearity are specified by various parameters such as Harmonic Distortion (HD), gain compression (1-dB compression point), cross-modulation and intermodulation distortion (IIP_2, IIP_3).

3.3 Receiver Front-End Architecture

In order to achieve the highest level of simplicity, we have chosen a direct-conversion architecture for the front-end. Fig. 3.1 shows the block diagram of the circuit; the key building blocks include a low-noise amplifier, a demodulator, and a 2nd-order low-pass filter. The detailed design considerations for these blocks will be discussed in later sections.

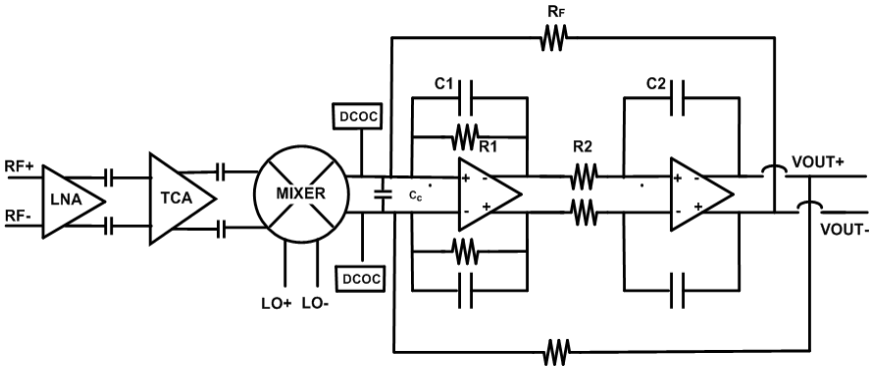


Figure 3.1: Front end Block Diagram

3.3.1 Target Specification

Targeted Specification for full system shown in Table 3.2.

Table 3.2: Full system specification of main path receiver

Parameters	Full System
Conversion Gain	$>$ 30
Bandwidth	0.3G - 3G
IF frequency	5 MHz
S11(dB)	$<$ -10
NF(dB)	$<$3
$CP1dB(dBm)$	$>$ -29
IIP3	$>$ -10

Parameters	LNA	Mixer
Conversion Gain	$>$ 15	$>$ 15
Bandwidth	0.3G - 3G	0.3G - 3G
IF frequency	-	5MHz
S11(dB)	$<$ -10	-
NF(dB)	$<$2	$<$2
$CP1dB(dBm)$	$>$ -5	$>$ -10
IIP3	$>$ 0	$>$ -5

3.4 Circuit Implementations

3.4.1 Wide Band Low Noise Amplifier (LNA)

In this section we will discuss detailed implementations of the front-end, covering all the major building blocks. The overall gain, noise figure and linearity requirement of a receiver front-end are partitioned and appropriate values of the same are assigned to individual sub-blocks such as LNA, mixer etc. Hence, framing specifications for LNA is completely dependent on receiver specifications and the successive sub-blocks in the receiver. Hence, a review of recently reported state of the art wide-band LNAs is done and the same is listed in Table 3.3.

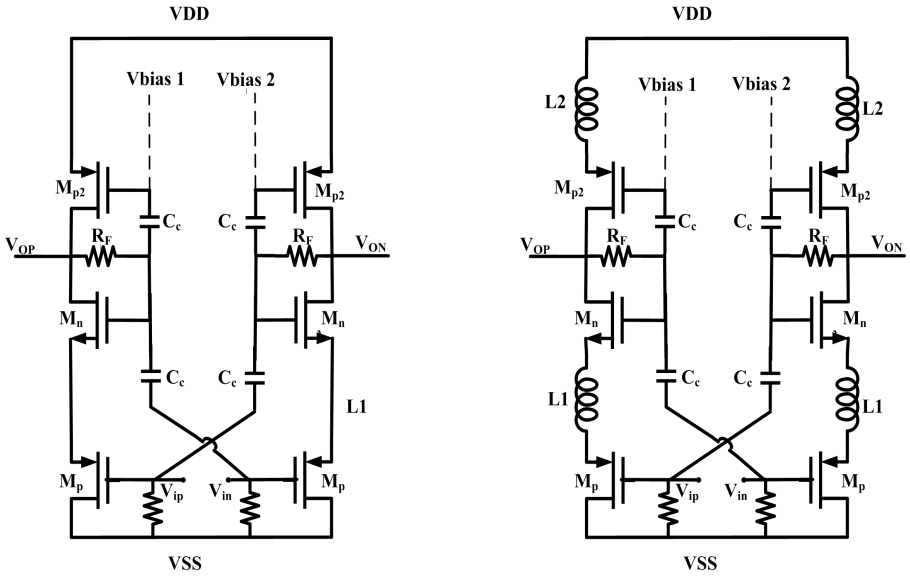
Table 3.3: Review of recent wideband LNA

Ref.	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)	Topology
[34]JSSC 2017	0.1 - 2	17.5	<-10	2.9 - 3.5	10.6 - 14.3	2.2	21.34	180	Complementry NMOS PMOS pair
[35] TCASII 2007	0.2 – 3.8	11.2	<-10	2.55-2.85	-2.7	1.2	1.9	65	dual capacitive cross-coupling
[36]ASSCC 2007	0.05 - 0.860	15	<-15	2.5	8.5	1.8	7.2	180	NMOS load and an extra signal feed -forward and noise-canceling path
[37]JSSC 2011	0.1 - 2.3	21	<-8	1.7 (dSB)	-1.5	1.8	18	90	Composite NMOS/PMOS pair
[38]MTT-S 2011	0.7 - 2.7	17.3	<-8	2 (dSB)	5	1.8	17.1	180	Common gate LNA with noise cancellation

The main issue concerning the broadband amplifier topologies is their inferior noise performance and wide band input matching for radio applications. A noise cancellation technique usually applied to a shunt-shunt feedback amplifier [39] to reduce the amplifier thermal noise figure below 3 dB, while maintaining broadband impedance matching from 2 to thousands of MHz and voltage gain of 20 dB. Further CG-CS noise canceling LNA came in picture. It cancels noise by introducing two stage. Various topology of LNA has been listed in Table 3.3. So composite transistor pair is better choice for wide band with low noise. This chapter will take on this task and analyze the noise cancellation with composite NMOS/PMOS cross coupled transistor pair in detail.

3.4.1.1 Composite Transistor Pair Bandwidth Enhanced Low noise amplifier (LNA)

Fig. 3.2(b) shows the modified proposed structure of LNA. The LNA core utilize the composite NMOS/PMOS transistor pair configuration. In this configuration, LNA incorporates a composite NMOS/PMOS cross-coupled transistor pair [37] techniques to increase the amplification while partially cancelling the noise generated by the input transistors. Proposed LNA gain bandwidth and input matching is enhanced in the form of inductive degenerative composite NMOS/PMOS cross coupled transistor pair, noise figure is improved by using low threshold voltage MOS (LVT CMOS). A source follower buffer is added for output matching and measurement purposes.



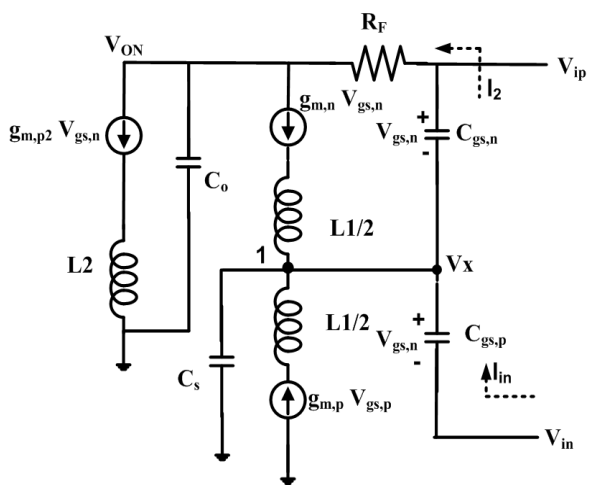
(a) Composite transister pair LNA [37]

(b) Modified structure of Low Noise Amplifier

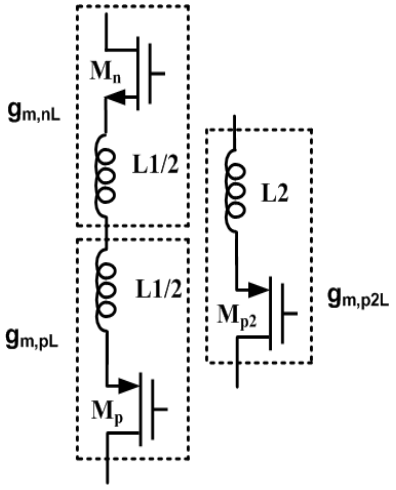
Figure 3.2: Proposed struture of LNA

3.4.1.1.1 Input Matching Analysis The input impedance $Z_{in,x}$ of Fig. 3.2(b) is derived using the half circuit small signal model. Small signal model of the proposed LNA is given by Fig. 3.3(a). By applying KCL in node 1

$$I_{in} = (V_{ip} - V_X)/(sC_{(gs,n)}) + V_X/sC_s - g_{(m,pL)}V_{(gs,p)} - g_{(m,nL)}V_{(gs,n)} \tag{3.4}$$



(a) Equivalent half circuit small signal model to find the input impedance of proposed Low Noise Amplifier



(b) Inductive degeneration of NMOS and PMOS

Figure 3.3: Equivalent small signal model of LNA

$$I_{in} = (V_{ip} - V_X)/(sC_{(gs,n)}) + V_X/sC_s - g_{(m,pL)}(V_{in} - V_X) - g_{(m,nL)}(V_X - V_{ip}) \tag{3.5}$$

$$I_2 = (V_{ON} - V_{ip})/R_F = g_{(m,nL)}V_{(gs,n)} = (V_X - V_{ip})/(sC_{(gs,n)}) \tag{3.6}$$

$$V_x = V_{in} - I_{in}sC_{(gs,P)} \tag{3.7}$$

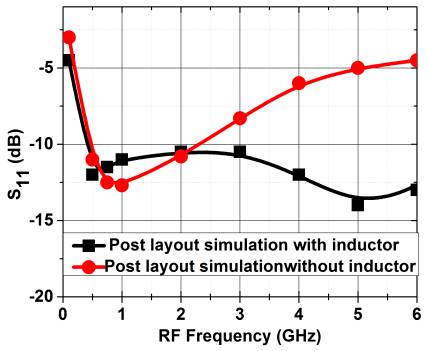
$$\frac{V_{in}}{I_{in}} = Z_{in} = \frac{1}{\frac{1+A_v}{R_F||1/sC_{gd,n}} + \frac{s(C_{gs,p}+C_{gs,n})(2g_{m,nL}+sC_s)}{g_{m,nL}+gm,pL+sC_s}} \tag{3.8}$$

Where while C_o and C_s are the output and source paracitics as shown in Fig. 3.3(a) and g_{meffL}, g_{mpL}, g_{mpL} and A_v are given in (3.9), (3.11), (3.10), (3.24) and L_1=L_2=L

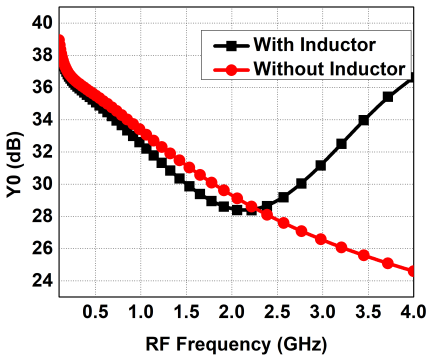
$$g_{meff_L} = \frac{g_{m,nL} * g_{m,pL}}{g_{m,nL} + g_{m,pL}} \tag{3.9}$$

where $g_{m,nL}$ and $g_{m,pL}$ are the transconductance of NMOS and PMOS transistor with inductive degeration as shown in Fig. 3.3(b) , respectively.

$$g_{m,nL} = \frac{g_{m,n}}{1 + s * L * g_{m,n}} \tag{3.10}$$



(a) Simulated S_{11} of LNA with and without inductor



(b) Simulated Z_{in} (Y_0) with and without inductor

Figure 3.4: Simulated S_{11} and Z_{in} of proposed LNA

$$g_{m,pL} = \frac{g_{m,p}}{1 + s * L * g_{m,p}} \tag{3.11}$$

Similarly g_{Mp2}

$$g_{Mp2L} = \frac{g_{m,p2}}{1 + s * L * g_{m,p}} \tag{3.12}$$

Input matching S_{11} of proposed LNA circuit is compared with and without L_1 and L_2 by simulation shown in Fig. 3.4(a). Composite NMOS/PMOS cross coupled transistor pair Fig. 3.2(a) incorpates resistive input matching in which C_{gs} limits the bandwidth. However, by introducing an inductor (L_1) at source of NMOS/PMOS bandwidth is improved and the effect of C_{gs} is minimized. By plotting the input impedance of Fig. 3.2(a) and Fig. 3.2(b) in Fig 3.4(b), it is clear that g_{mpL} and g_{mpL} trying to reduce Z_{in}, thus improved $S_{11} = |Z_{in}\text{-}Z_s|/|_{Zin} + Z_s|$ is reflected in Fig. 3.4(a). The LNA has designed to achieve an S11 < -10 dB from 0.3 GHz to 3 GHz. It is clear from Fig. 3.4(a) that the inductor significantly improves the input matching. Thus, L_1 and L_2 helps in achieving wideband input matching and same is listed in Table3.4.

Table 3.4: Input reflection with and without inductor

	Without inductor	With inductor
S11 (dBm)	< -11	< -11
Operating bandwidth (GHz)	0.3 - 2.3	0.1- 6

3.4.1.1.2 Noise Analysis The different noise sources affecting the overall noise figure of LNA are shown in Fig. 3.5 where only the noise contributor of half of the circuit is shown. Equivalent circuit of inductor is shown by inductor with series resistor r_l, but effect of r_l is very small so it is neglected. The effect of parasitic capacitances will be ignored to simplify the analysis and because noise figure is important in the midband of operation. we can break this circuit in further parts to analyze.

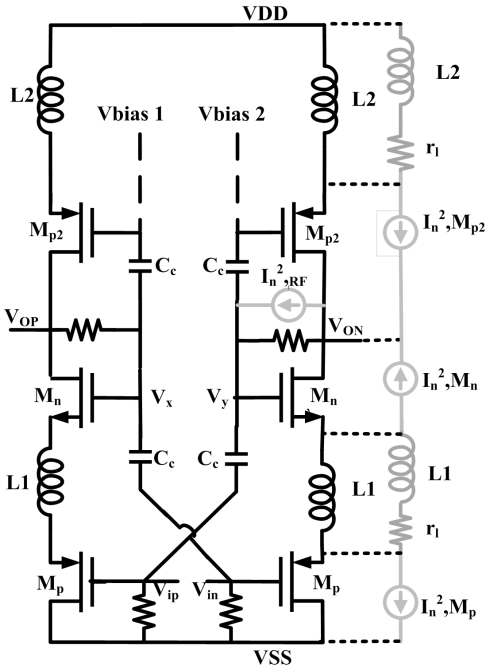


Figure 3.5: Noise equivalent of Low Noise Amplifier

First, let us qualitatively analyze the proposed noise cancellation principle. Differential configuration amplifies the differential voltage and rejects the common mode noise. The composite NMOS/PMOS transister is used as the basic cell to reduce the overall noise figure of LNA. The amplification of the input signal is demonstrated by considering the half-circuit model. In this model, input signals to gates of M_{nL} and M_{pL} and carry different polarity $V_{ip} - V_{in}$ leading to an amplification of the input signal.

Considering the noise generated by the NMOS and PMOS transistors, the cross connection leads to partial noise cancellation of the generated noise. The partial cancellation is clarified qualitatively for the proposed architecture, the noise current due to the right NMOS transistor

$I_{n,M_{nL}}$ is considered. The noise current produces an output noise voltage, V_{ON}. Then, V_{ON} generates a noise voltage at nodes V_X and V_Y. These two voltages drive the left section and produce an output noise voltage, V_{OP} , which is a fraction of V_{ON}. Due to the cross connection, V_{OP} carries the same polarity as, V_{ON} and thereby the differential output noise voltage and noise figure are reduced. Similarly the noise generated by M_{pL} is partially canceled. In the conventional case, V_{ON} and V_{OP} carry different polarities, and therefore the conventional LNA with resistive feedback has higher noise figure. Thermal noise and flicker noise of MOS and resistance are assumed from standard model and are defined as in (3.13) (3.14)

Noise current of M_{nL} due to thermal noise

$$i_d^2 = 4kT\gamma * g_{m,nL} * \Delta f \tag{3.13}$$

Noise current of M_{nL} due to flicker noise

$$i_n^2 = \frac{k}{(C_{OX}WL)} * 1/f * g_{m,nL}^2 = \frac{k}{C_{OX}L^2} * 1/f * I_D \tag{3.14}$$

Noise current of M_{nL} due both to thermal and flicker noise

$$i_{Mn}^2 = 4kT\gamma * g_{m,nL} * \Delta f + \frac{k}{C_{OX}L^2} * 1/f * I_D \tag{3.15}$$

k is Boltzmann constant, γ and $K_{(F,n)}$ are the thermal and flicker noise factor respectively. I_D is the DC current C_{OX} is the oxide capacitance per unit area, L is the channel length of MOS.

Similarly Noise current of M_{pL} due both to thermal and flicker noise

$$i_{Mp}^2 = 4kT\gamma * g_{m,pL} * \Delta f + \frac{k}{C_{OX}L^2} * 1/f * I_D \tag{3.16}$$

$$i_{(n,R_L)}^2 = \frac{4kT}{R_L}\Delta f \tag{3.17}$$

The input referred noise voltage due to the thermal noise of RF

$$i_{n,R_F}^2 = \frac{4kT}{R_F} * |A_I, R_F|^2 \tag{3.18}$$

where

$$A_I = (-g_m + 1/R_F) * (R_F||R_D) \tag{3.19}$$

$$v_{in,R_F}^2 = \frac{1}{2}(1 + \frac{1}{g_{m,nL}R_s})^2 \frac{R_s^2}{R_F} * kT\Delta f \tag{3.20}$$

$$\begin{aligned} NF = 1 + \frac{\gamma/g_m, nL + \gamma/g_m, pL}{2 * R_s} + \frac{\frac{K_{F,n}}{g_{m,nL}^2 * L_n^2} + \frac{K_{F,p}}{g_{m,pL}^2 * L_p^2} * I_{DC}}{8kTfC_{ox}R_s} \\ + \frac{1}{2}(1 + \frac{1}{g_{m,effL}R_s})^2 \frac{R_s^2}{R_F} + \frac{1}{2g_m, effL^2 * R_L * R_s} \end{aligned} \tag{3.21}$$

Transistor M_{p2L} also provides an additional transconductance to increase the overall gain of the LNA. Increasing the overall gain helps to reduce the noise contribution of the load and feedback resistances, and therefore lowering the overall noise figure. With the additional transistor total noise figure is

$$\begin{aligned} NF = 1 + \frac{(2\gamma_n * g_{m,effL}^2)}{g_{m,n}R_s(2g_{m,effL} + g_{m,p2L})^2} + \frac{2\gamma_p * g_{m,effL}^2}{g_{m,p}R_s(2g_{m,effL} + g_{m,p2L}{}^2)} \\ + \frac{\gamma_p g_{m,p2L}}{R_s(2g_{m,effL} + g_{m.p2L})^2} + \frac{1}{2}[1 + \frac{2}{2 * (g_{m,effL} + g_{m,p2L})R_s}]^2 * \frac{R_s{}^2}{R_F} \end{aligned} \tag{3.22}$$

Where g_{meffL}, g_{mpL} and g_{mpL} are given in (3.9) , (3.11), (3.10)

Effect of inductor on noise figure is negligible as inductor doesn't introduce any noise but at higher frequency gain flatness is increasing, so noise reduces by 0.1dB as shown in Fig. 3.6 and compared with Fig. 3.2(a). To provide better headroom in cascode topology, regular threshold voltage MOS (RVT MOS) is replaced with low threshold voltage MOS (LVT MOS). After replacing RVT MOS with LVT MOS to provide equivalent g_m (maintaining input matching and

gain BW), aspect ratio of LVT MOS is reduced. By looking equation of channel thermal noise as given (3.23) [40], thermal noise current is proportional to width. Thus it is concluded that thermal noise will decrease as width of the MOS decreases. By decreasing width while maintaining same g_m achieved noise figure with LVT MOS is 1.2dB can be seen by Fig. 3.6 and tabulated in Table3.5. Fig. 3.7 shows the individual noise contributors with LVT MOS and RVT MOS. Hence it is concluded LVT MOS contributes less noise.

$$i_d{}^2 = 4kT\mu * C_{ox}\frac{W}{L}\frac{2}{3}[\frac{3(V_{GS}-V_T)V_{DS}-3(V_{GS}-V_T)^2-V_{DS}{}^2}{2(V_{GS}-V_T)-V_{DS}}] \tag{3.23}$$

Table 3.5: Simulated Noise figure summary with RVT CMOS and LVT CMOS of LNA

	Current consumption	Noise Figure
RVTMOS	11.6	1.6
LVTMOS	12.5	1.2

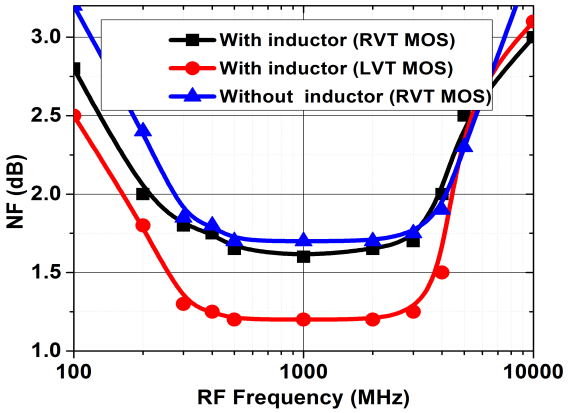


Figure 3.6: Simulated Noise Figure with LVT MOS and RVT MOS of LNA

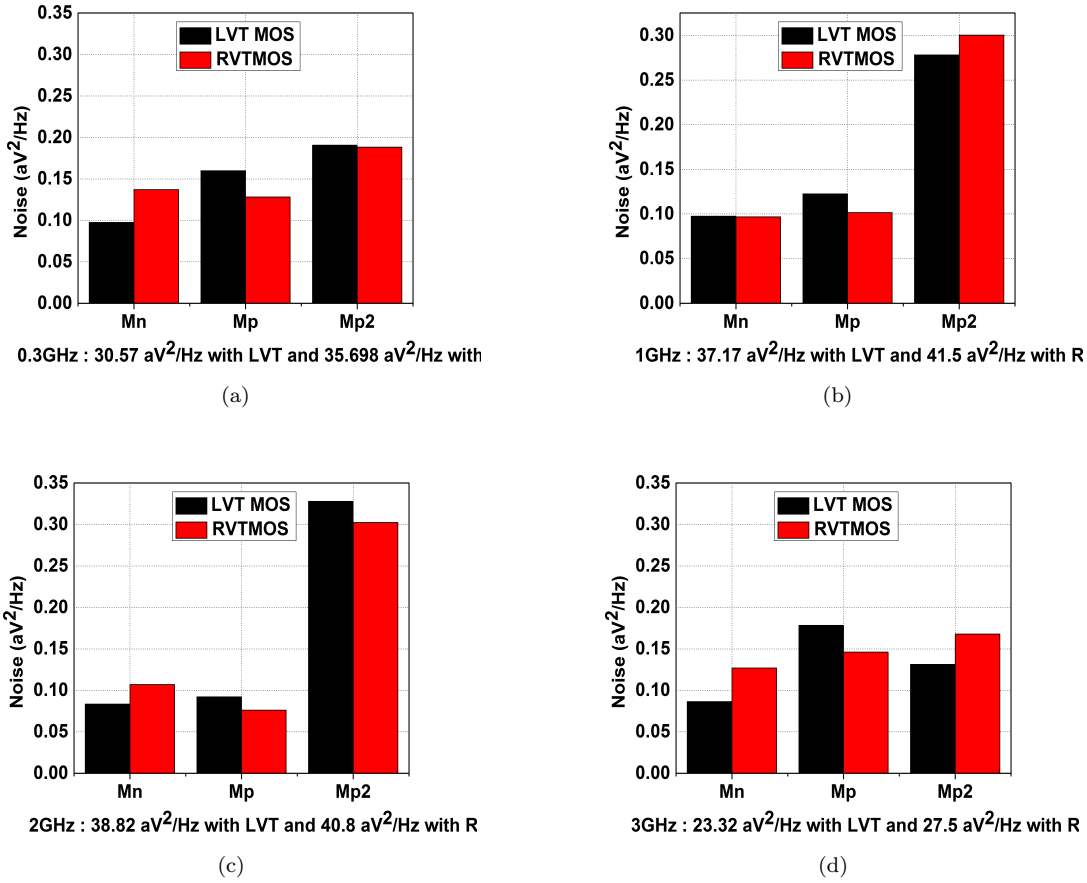


Figure 3.7: Noise contribution of individual MOS of LNA at different frequency

3.4.1.1.3 Gain Analysis Analytical expression for voltage gain: The transfer funtion of the proposed LNA in Fig. 3.2(b) is calculated using the half circuit small signal model represented in Fig. 3.3(a).

$$A_v(s) = \frac{V_{op} - V_{on}}{V_{in} - V_{ip}} = \frac{-(A_{v,mid} * (1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p0}}) * (1 + \frac{s}{\omega_{ps}})} \tag{3.24}$$

where

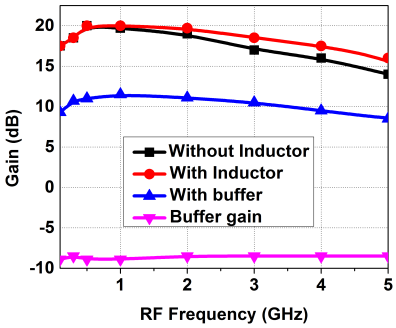
$$A_{(v,mid)} = (2g_{m.effL} + g_{m,P2L})(R_F||r_O) \tag{3.25}$$

$$\omega_z = \frac{2g_{m,pL}}{2C_{gs,p} + C_s} \tag{3.26}$$

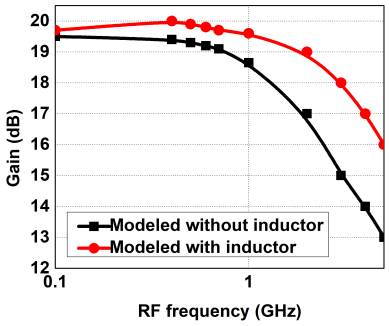
$$\omega_{p0} = \frac{1}{C_0 * (R_F || r_O)} \tag{3.27}$$

$$\omega_{ps} = \frac{g_{mnL} + g_{mpL}}{C_{gs,p} + C_{gs,n} + C_s} \tag{3.28}$$

where$A_{v,mid}$ is the mid-band gain, ω_{po} is the pole at the output, and ω_{ps} and ω_z are due to the parasitic capacitances $C_{gs,n}, C_{gs,p}$ and C_s. $C_{gs,n}, C_{gs,p}$ are the gate source capacitance of the NMOS/PMOS transistor, while C_o and C_s are the output and source paracitics as shown in Fig. 3.3(a).



(a) Bandwidth extension with inductor and loss due to buffer of LNA



(b) Modeled conversion gain of LNA based on (3.24)

Figure 3.8: Simulated and modeled conversion gain of LNA

The conversion gain of proposed LNA is compared in simulation as well modeled using (3.24). Fig. 3.8(a) and Fig. 3.8(b) shows the simulated conversion gain and modeled based on (3.24) with and without inductor. As shown in Fig. 3.8 the proposed architecture significantly improves gain banwidth. It is clear from Fig. 3.8(a) and Fig. 3.8(b) that L_1 and L_2 helps in achieving wideband gain flatness. The LNA has designed to achieve 20dB gain from 0.3 GHz to 3 GHz. Thus it is concluded that proposed architecture improves gain flatness, noise and input reflection. A source follower buffer is added for output matching and measurement purposes. Source follower

has around 8-10dB loss.

3.4.2 Down Conversion Mixer

Down conversion mixer conceptual diagram is shown in Fig. 3.9. In this section we will discuss detailed design implementations of the down conversion mixer, covering all the major building blocks (transconductance amplifier, switches, transimpedance amplifier) and analysis. Mixer is the most nonlinear block in receiver path. The overall gain, noise figure and linearity requirement of a receiver front-end also dependent on subblock (mixer) performance, so choice of mixer plays an important role.

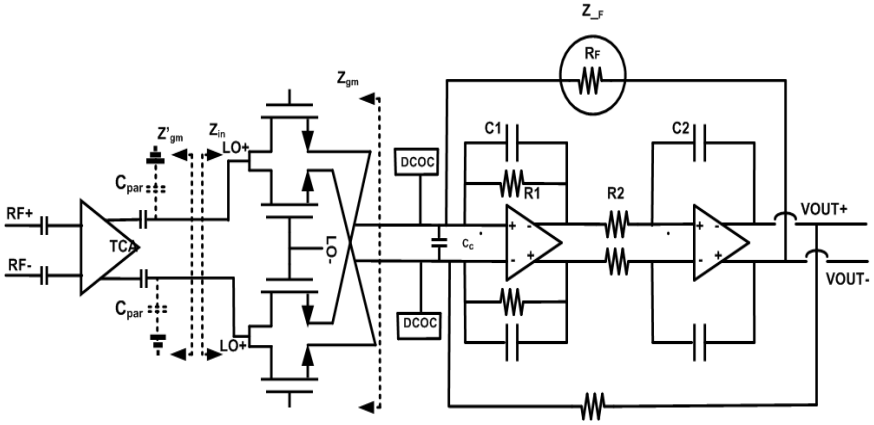


Figure 3.9: Down Conversion Mixer conceptual diagram

Table 3.6: Review of recent down conversion mixer

Ref.	Frequency (GHz)	A_v (dB)	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)
[41] CICC 2016	0.7 - 2.5	35	10	7	1.5	30	130
[42] RFIC 2008	1.35-2.3	24	8	9	2	10	180
[43] JOS 2013	0.7 - 2.3	21	10.6	9	1.8	9.9	180
[44] ISCAS 2013	0.9, 1.9-2.5	13	13.7	10.7-13.8	1.2	8.04	65
[45] MTT-S 2015	0.7 - 2.6	8/14/20/26)	9.1	8.5	1.8	8.82/14.04	180

Hence, state of the art of recently reported down conversion mixer is listed in Table 3.6. The main issue concerning the down conversion mixer topologies is their nonlinearity. After reviewing and comparative study of various papers, Conventional Fully differential TCA followed by Switching quad followed by Tow Thomas Biquad has been found the Preferable structure. This section will take on this task and analyze the down conversion mixer configuration in details

3.4.2.1 Transconductance Amplifier

Multiple Gated Linearity Enhancement Techniques

Nonlinearity in receiver circuits, such as low-noise amplifiers (LNAs) and mixers, is directly related to immunity to the various interferences such as harmonic generation, gain compression, desensitization, cross modulation and intermodulation. Among various distortions, even-order distortion caused by even-order nonlinearity can easily be reduced by adopting a differential signal processing architecture. It is difficult to reduce odd-order distortion. Among odd-order distortions, the third-order intermodulation distortion (IMD) is the most dominant nonlinearity component. The performance measure for this nonlinearity is usually expressed by the third-order input intercept point (IIP_3), since the third-order intercept point (IP_3) is usually proportional to DC power consumption.

Several circuit techniques have been proposed to improve the (IIP_3) of RF amplifiers. Most of them are based on negative feedback circuits. One of the most famous ones is series feedback using source degeneration by resistor or inductor [46]. Source degeneration using an inductor is very plausible because it does not increase the noise figure. Another good example of CMOS parallel push pull architecture [47] or g_m boosted cross coupled push pull architecture. Even though these methods are effective to enhance (IIP_3), they have problems of gain reduction [48]. Actually, the enhancement in linearity is the result of the gain reduction. Although IIP_3 can be improved by the differential circuit technique, IIP_3 is ultimately limited by the MOSFET transconductance nonlinearity itself. In this regard, there have been several attempts to reduce third-order transistor transconductance nonlinearity.

One technique that can be used for building block linearization is by using multiple gated transistors. MGTR is an effective way to linearize the common-source (CS) MOSFET without increasing DC power consumption [49]- [50]. In general, the drain current of a common source MOS transistor (assuming a memory-less non-linearity) is expressed as:

$$i_{DS} = I_{DC} + g_m * v_{gs} + \frac{g'_m * v_{gs}^2}{2!} + \frac{g''_m * v_{gs}^3}{3!} F1 + ... \tag{3.29}$$

Here, v_{gs} is a small-signal gate-to-source voltage and g'_m, g''_m indicates first and second order transconductance with respect to v_{gs}. It is well known that the coefficient in (3.29) plays an important role in determining the IMD_3 of an RF amplifier. In MGTR, these coefficient could be minimized by linearly superposing several CS FET transistors with proper bias and size in parallel [49].

Fig. 3.10. shows a typical simulated current and its derivative (g_m, g'_m and g''_m) characteristics of an NMOS. The figure shows that the g''_m goes to the positive peak value in the subthreshold region, then crosses zero and shows a negative peak value at the gate voltage higher than V_{th}. To reduce the DC power consumption without losing the RF gain, the gate bias voltage of the RF amplifier is usually biased at overdrive (V_{gs} - V_{th}) in the range between 0.1 and 0.4 V. Unfortunately, the g''_m in this bias region has a negative peak value (as shown in Fig. 3.10(a), which significantly degrades the linearity of an amplifier.

Fig. 3.10(b), M1 is biased at V_{gs}, and M2 is biased at V_{gs}-V_{shift}, so the transfer characteristic curve for M2 is shifted to the right by the amount of V_{shift}. Once the bias points for M1 and M2 are determined, the amount of compensation for the value of g''_m can be chosen by adjusting the width of M2, resulting in a Multi-Gate Transistor (MGTR) amplifier, as shown in Fig. 3.10(c).

In the MGTR amplifier, however, this negative peak of the main transistor(MT) can be cancelled by the positive peak value of a properly sized auxiliary transistor, whose transfer characteristic is shifted to the right by changing either the gate bias or the threshold voltage as shown in Fig. 3.10(c). Note that, because auxiliary transistor is biased in subthreshold regime, this linearization method does not consume any extra power.

Circuit implementation The mixer consists of a transconductance (g_m) stage, a switching quad, and an RC feedback transimpedance amplifier at the output which is Tow Thomas biquad (second order filter). The mixer g_m stage is shown in Fig. 3.11 and is again a complementary pair, with both NMOS and PMOS input devices. A complementary input increases the current efficiency of the circuit and reduces the overall IM_2 contribution of the stage due to the IM_2 cancellation mechanism, as discussed above. The use of multi-gated input pairs allows tuning to find the optimal operating points that results in higher performance of the circuit with almost

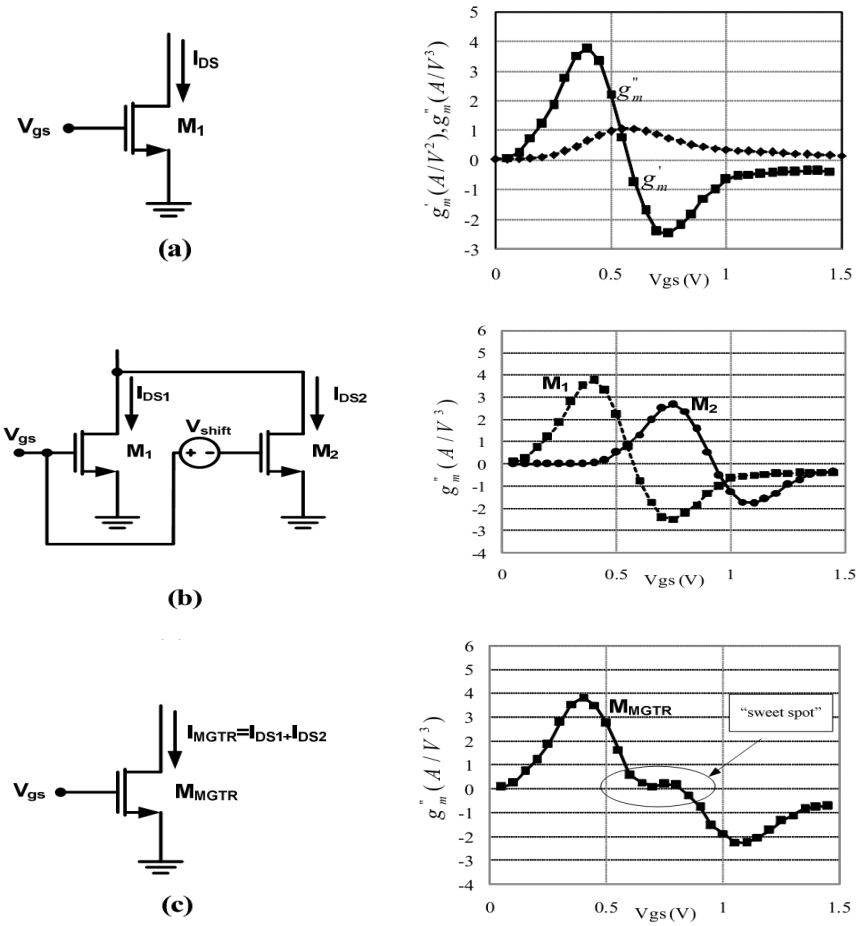


Figure 3.10: Multigate Transistor Concept

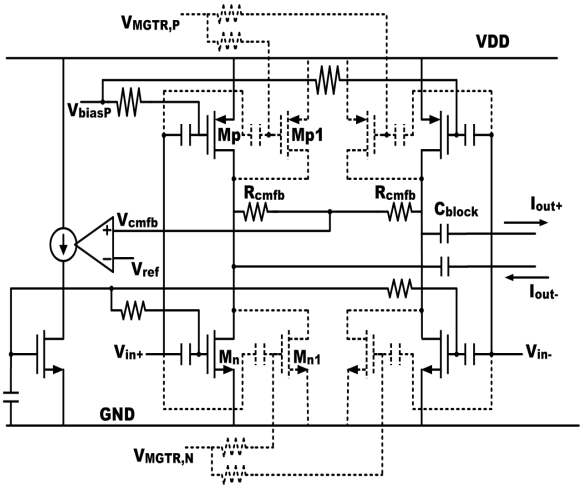


Figure 3.11: Transconductance amplifier of down conversion mixer

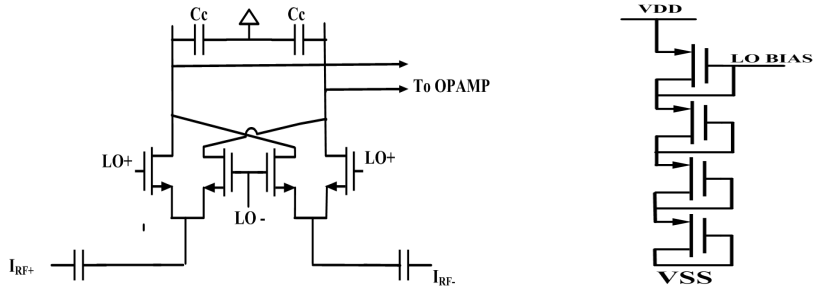
the same bias current. Both PMOS and NMOS input stages use balanced input devices with no tail current source in order to increase voltage headroom.

3.4.2.2 Switches

The main advantage of the passive switching is that it does not dissipate static power. More importantly, passive mixers have very low distortion, low 1/f noise, and no shot noise. Since the high frequency noise is entirely thermal, the noise figure depends on the conversion loss. The resistance of the switch is non-linear but still their linearity performance is better than an active mixer. Passive mixers are divided into current mode passive mixer and voltage-mode passive mixer [51]. Current Commutating passive mixer is preferred over voltage mode because of better linearity.

The switches consist of four transistors forming a double-balanced structure as shown in Fig. 3.12(a). LO signals are AC coupled via capacitors The DC bias level at the gate of the switches is set at a level where the switches are operating near the threshold of conduction in order to achieve the lowest on-resistance while preventing overlapping on-periods. The switches should be sized big enough in order to minimize the on-resistance. The overlapping on-periods of the switches result in lowered conversion gain and increased flicker noise from the LO port, while an overlapping off-period will result in linearity degradation. To ensure that the bias voltage

tracks with process variation, it is generated by PMOS stacked circuit, as shown in Fig. 3.12(b). As mentioned in the previous section, the common-mode voltage level at the drains and sources of the switches is chosen to be Vdd/2 in order to obtain the highest voltage headroom at the output of the transconductance stage. Assuming the highest allowable gate voltage is Vdd, the highest overdrive voltages of the switches will be Vdd-Vdd/2-Vth. If the voltage headroom is not a constraint, common-mode voltage level can be reduced to allow higher LO voltage swing and higher overdrive voltage of the switches (as high as Vdd/2 for the overdrive). Higher overdrive voltage results in lower average on-resistance of the switches and increases linearity, gain, and noise performance of the mixer. Shunt capacitor Cc at the mixer output nodes to ground is the high frequency compensation capacitance including LO leakage and generated LO harmonics.



(a) Quad Switch Configuration

(b) process independent bias for local oscillator signal

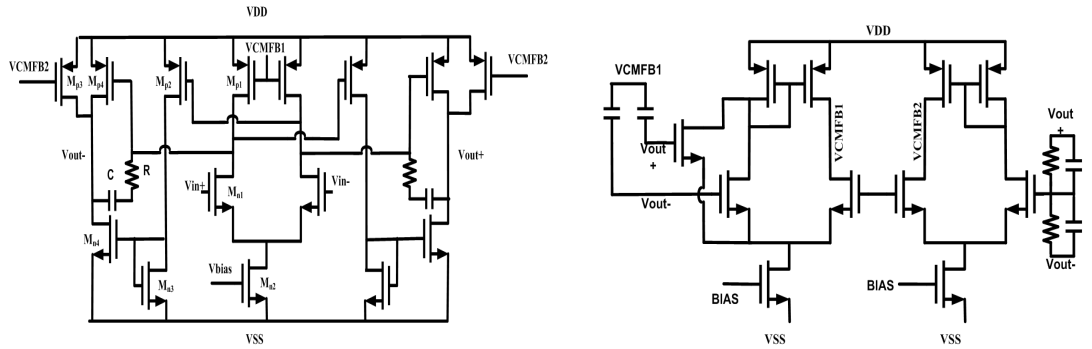
Figure 3.12: Switching stage and its bias generation

3.4.2.3 Transimpedance Amplifier

OTA and feedback circuit

The switching quad output current directly feeds to the Tow Thomas biquad filter (TIA) as shown in Fig 3.9, which performs the I/V conversion and also realizes a pair of complex poles. The biquad TIA outperforms the commonly used first order TIA in the following three aspects. First, there is less in-band gain loss due to the complex response. Second, it is demonstrated in [52] that for the biquad configuration, the second stage in the loop enhances the overall loop gain compared with the single stage active-RC filter sections. As a result, the nonlinearity caused by operational amplifiers is suppressed more and better linearity is achieved. Last but not least,

for the biquad configuration, the blockers can be suppressed more effectively before the first high voltage swing node at the TIA output. The biquad TIA shown is nothing but Tow- Thomas biquad topology. This Tow-Thomas-like biquad topology is chosen for its parasitic insensitive property and ease of corner tuning.



(a) OTA (b) OTA CMFB

Figure 3.13: Two stage OTA used for TIA

The transfer function can be expressed as

$$T_{LPF}(s) = \frac{H * \omega^2}{s^2 + \frac{\omega}{Q} * s + \omega^2} \tag{3.30}$$

$$T_{BPF}(s) = \frac{H * \frac{\omega}{Q} s}{s^2 + \frac{\omega}{Q} * s + \omega^2} \tag{3.31}$$

$$H = g_{mTCA} * R_F \tag{3.32}$$

where the cut-off frequency ω and quality factor Q are

$$\omega = \sqrt{\frac{1}{R_2 R_F C_1 C_2}} \tag{3.33}$$

$$Q = R_1 \sqrt{\frac{{R_1}^2 C_1}{R_2 R_F C_2}} \tag{3.34}$$

Tow Thomas biquad, amplifier consists a two stage OTA shown in Fig. 3.13(a) and CMFB shown in Fig. 3.13(b). First stage to provide high gain and second stage for high swing. So that structure can obtain both, high output swing and low input referred noise. Transimpedance amplifier is used to convert current to voltage output in passive mode operation. The TIA stage serves as load and anti-aliasing filter for the passive mixer. A very low impedance in the desired signal frequency band is created at the TIA input by the operational amplifier feedback loop.

3.4.3 Analysis of Down Conversion Mixer

3.4.3.1 Conversion gain of passive mixer

Conversion gain of mixer is defined as

$$\frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} * g_m * R_F \tag{3.35}$$

where R_F are feedback resistance of tow thomas biquad filter, g_m is the transconductance of transconductance amplifier and the factor 2/Π is related to the first harmonic amplitude of the periodically time varying transfer function .

3.4.3.2 Noise sources in passive mixer architecture

Major noise sources in this architecture are, the input transistors, the transimpedance amplifier, the feedback resistors, and the transistors in the switching quad. The 1/f noise in the switching quad depends on the amount of current flowing through the switches. Since there is a very small DC bias current flowing through the switches, 1/f noise from the switching quad can be made negligibly small. Noise at the output of the mixer from each of the major noise sources is:

$$V^2{}_{n,out}(f_{RF}, f_{IF})_{gm} = (4kT\gamma * g_{ds0})\beta^2 |R_f(f_{RF})|^2 \Delta f \tag{3.36}$$

$$V^2{}_{n,out}(f_{RF}, f_{IF})_{switches} = \frac{4kT}{R_{ON}} | \frac{R_{ON}}{R_{ON} + Z_{gm}(f_{RF})} |^2 * \beta^2 * |R_F(f_{RF})|^2 \Delta f \tag{3.37}$$

$$V^2{}_{n,out}(f_{RF}, f_{IF})_{opamp} = V_{n,opamp}{}^2 | 1 + \frac{2R_F(f_{RF})}{Z_{gm}(f_{RF})} |^2 \tag{3.38}$$

$$V^2{}_{n,out}(f_{RF}, f_{IF})_{R_F} = 4kTR_F\Delta f \tag{3.39}$$

where γ is process-dependent, β^2 is a constant representing switching activities, including noise folding effects, and equals $\Pi^2/8$ under the assumption of perfect-square wave switching. $V^2{}_{opamp}$ is the operational amplifier's input-referred voltage noise, R_{ON} is the average on-resistance of the switches, and Z_{gm} is the effective impedance looking into the switches from the transimpedance amplifier as shown in Fig. 3.9. If the current is small and the transistor is biased to have low average on-resistance, the noise contribution from the switches to overall noise performance is negligible. If we exclude the noise from the source and the switching quad, the total added output spot noise in the mixer can be estimated as:

$$V^2{}_{n,out}(f_{RF}, f_{IF}) = (4kT\gamma * g_{ds0})\beta^2 |R_f(f_{RF}|^2 \Delta f + V_{n,opamp}{}^2 | 1 + \frac{2R_F(f_{RF}))}{Z_{gm}(f_{RF}} |^2 + 4kTR_F\Delta f \tag{3.40}$$

Dividing the output noise by the voltage gain of the mixer, the input referred voltage noise is:

$$V^2{}_{n,out}(f_{RF}, f_{IF}) = \frac{(4kT\gamma * g_{ds0})\beta^2 |R_f(f_{RF})|^2 \Delta f}{(\frac{2}{\pi})^2 g_m{}^2 R_F{}^2} + \frac{V_{n,opamp}{}^2 | 1 + \frac{2R_F(f_{RF})}{Z_{gm}(f_{RF})}|^2}{(\frac{2}{\pi})^2 g_m{}^2 R_F{}^2} + \frac{4kTR_F\Delta f}{(\frac{2}{\pi})^2 g_m{}^2 R_F{}^2} \tag{3.41}$$

An interesting observation from 3.41 is that the input-referred noise increases when Z_{gm}

decreases. If Z_{gm} is dominated by the parasitic capacitance C_{par}.

$$Z_{gm}(f_{RF}) = \frac{1}{4f_{LO}C_{par}} \tag{3.42}$$

where f_{LO} is the LO frequency, which is close to f_{RF} for direct conversion receivers. Noise contributions from the transimpedance amplifier become significant at higher input frequency, and increase with C_{par}. In a narrowband design we can employ an inductor to tune out C_{par}, whereas in this broadband design it is important to reduce this capacitor as much as possible.

3.4.3.3 Linearity

Linearity performance in the mixer depends on: 1) the linearity of the voltage-to current conversion in the transconductance stage, 2) effects from the switching stage, as well as 3) the linearity of the transimpedance amplifier stage. The linearity of a transconductance stage can be achieved much better with careful sizing and moderate current consumption. In wideband designs, the linearity of this stage will be relatively flat as a function of operating and offset frequencies. The linearity of the transimpedance amplifier, however, depends strongly on the frequency offsets of the blocking signal from the carrier, as can be explained as follows. As depicted in Fig. 3.9, the transimpedance amplifier can be viewed as a current-feedback amplifier with feedback impedance R_F and driven by a current source with effective impedance Z_{gm}. Assuming an amplifier has a forward voltage transfer function of) $A(f)$, the total loop gain of this amplifier can be written as

$$T(f) = A(f) * \frac{Z_{gm}(f)}{Z_{gm}(f) + R_f(f)} \tag{3.43}$$

To get higher loop gain and a higher input-referred input intercept point, we need to maximize the open-loop linearity of A(f) as well as the loop gain. Due to frequency conversion in the switches, impedance $Z_{gm}(f)$ is approximately constant as a function of baseband frequency. R_F, however, follows 20 dB/dec decrease with baseband frequency since it is an RC network. If the magnitude and linearity of A(f) are relatively constant, loop gain increases with the frequency and results in a better linearity intercept-point of the circuits. Once the frequency increases to a point where the open-loop gain of the amplifier decreases, the loop-gain and linearity performance

of the circuit do not increase further. It is worth mentioning that the linearity of A(f) is not constant as a function of frequency, and it affects the overall linearity of the circuit as well. Since a passive mixer requires a high level of LO drives at the switches, a major concern in this architecture is the LO-RF leakage in the circuit which can degrade IIP_2 of the system due to finite IIP_3 of the front-end blocks.

3.5 Wide Band Receiver Taped Out Design

Core LNA and down conversion mixer: This receiver circuit is designed using UMC 65nm 1P9M2T0F1U RF CMOS technology in Cadence design environment and simulated with SpectreRF simulator. Physical verification is done in Mentor Graphics Calibre tools. Proposed LNA has noise cancellation with bandwidth enhanced techniques. Widths of each M_n, M_p, M_{p2} transistors are carefully chosen carefully to achieve optimum performance for input matching and gain. Inductor value is critical since it defines the gain bandwidth and input matching, a 2.29nH inductor is chosen for L_1, L_2. A 550Ω RNHR resistance is chosen for Feedback resistance (R_f). M_{p2} is used as a load in place of resistor to reduce noise. Fully differential LNA is design to minimize the noise figure. A source follower buffer is added for output matching and measurement purposes shown in FIg 3.14. The output buffer reduces the voltage gain by ≈ 9 dB and increases the noise figure by ≈ .6 dB. Table 3.7 summarize the component values of implemented LNA and buffer.

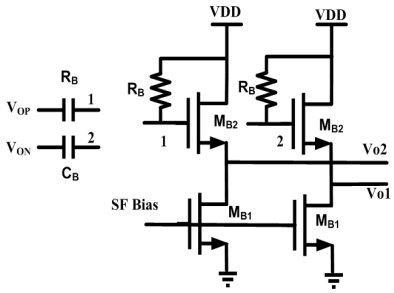


Figure 3.14: Circuit schematic of buffer used for output matching and measurement purpose of LNA

Further in down conversion mixer, a fully differential MGTR TCA followed by switching

Table 3.7: Circuit element values and transistor aspect ratio for the implemented LNA and Buffer

$(\frac{W}{L})_{M_n}$	$(\frac{W}{L})_{M_p}$	$(\frac{W}{L})_{M_{p2}}$	Rf	$L1, L2$	Cc
$(\frac{157.5um}{60nm})$	$(\frac{375um}{60nm})$	$(\frac{330um}{60nm})$	554.62Ω	2.29nH	20pF
$(\frac{W}{L})_{M_{B1}}$	$(\frac{W}{L})_{M_{B2}}$	R_B	C_B	LNA_{IBias}	I_{Buffer}
$(\frac{40um}{60nm})$	$(\frac{96um}{60nm})$	50KΩ	9.8pF	640uA	5mA

stage, and TIA is designed. On chip automatic tuning or compensation is not implemented in MGTR TCA design, the tuning capability is added to enable on-board tuning and to enable use of the front-end for future research in tuning algorithms. The tuning voltage can be adjusted manually during testing if required. An AC coupling capacitor is used at the output in order to ensure that low frequency IM2 tones will be blocked from entering later stages. Since, auxiliary transistor operates in weak inversion and suffers more from process variation effects, but biasing circuit designed in such a way to minimize process variation. All MOS dimension are given in Table.3.8. TCA output current is feeded to Switching quad with dimension $40\mu/60$n. Dimension of switching MOS is chosen to minimize on resistance. Switching quad output is coupled to biquad filter. IF voltage is built at the output of transimpedance amplifier after the RF current gets commutated in switching stage and passes to second order tow thomas biquad filtering. three stage OTA is designed for TIA. A source follower buffer is designed and added at the output for output matching and measurement purpose. LNA is designed at 1.5V supply voltage. Down conversion mixer is designed for 1.2V supply voltage. Differential buffer consumes $\sim$ 24mA current.

Table 3.8: Circuit element values and transistor aspect ratio of TCA

$(\frac{W}{L})_{M_n}$ Main transistor	$(\frac{W}{L})_{M_p}$ Auxiliary transistor	$(\frac{W}{L})_{M_{n1}}$ Main transistor	$(\frac{W}{L})_{M_{p1}}$ Auxiliary transistor
$(\frac{24um}{60nm})$	$(\frac{46.42um}{60nm})$	$(\frac{19.8um}{60nm})$	$(\frac{24um}{60nm})$

Table 3.9: Circuit element values and transistor aspect ratio of OTA

$(\frac{W}{L})_{M_{n1}}$	$(\frac{W}{L})_{M_{n2}}$	$(\frac{W}{L})_{M_{n3}}$	$(\frac{W}{L})_{M_{n4}}$	$(\frac{W}{L})_{M_{p1}}$	$(\frac{W}{L})_{M_{p2}}$	$(\frac{W}{L})_{M_{p3}}$	$(\frac{W}{L})_{M_{p4}}$	R,C
$(\frac{200um}{2m})$	$(\frac{328um}{2um})$	$(\frac{1.75um}{250nm})$	$(\frac{15um}{250nm})$	$(\frac{500um}{2um})$	$(\frac{21.97um}{60n})$	$(\frac{505um}{60n})$	$(\frac{100um}{60n})$	72Ω, 6.81pF

Bias Circuit: All bias voltages are generated internally to counter the process variation. All bias are generated using same technique as shown in Fig. 3.15. It is designed using current mirroring from constant current source. OPAMP 600mV is feeded from BGR. BGR consumes 78μA current. Bias core consumes 500μ current. All bias are generated by mirroring point A and B. Down conversion mixer bias circuit also designed same way. LNA bias generation consumes more current because LNA MOS dimensions are more.

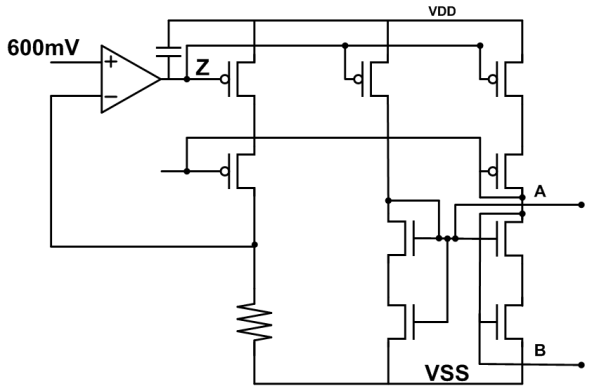


Figure 3.15: Schematic diagram of bias generation core

ESD Protection All I/O interface pads are attached with Electro Static Discharge (ESD) protection circuit. Generic PN junction diode based protection circuit is used for all signal pads (DC and RF) as shown in Fig. 3.15(a). Size of the protection diode is chosen by considering optimum trade-off between protection and performance. DC pads use higher width diodes facilitating high current flow, while RF pads use low width diode for reduced parasitic capacitance impact to the signal. ESD protection for VDD pad is designed as shown in Fig. 3.15(b). This protects the chip from any ESD event on VDD pad by making a momentary short circuit between supply and ground. For this reason, the short circuit MOS, M_{SH} has been chosen very large.

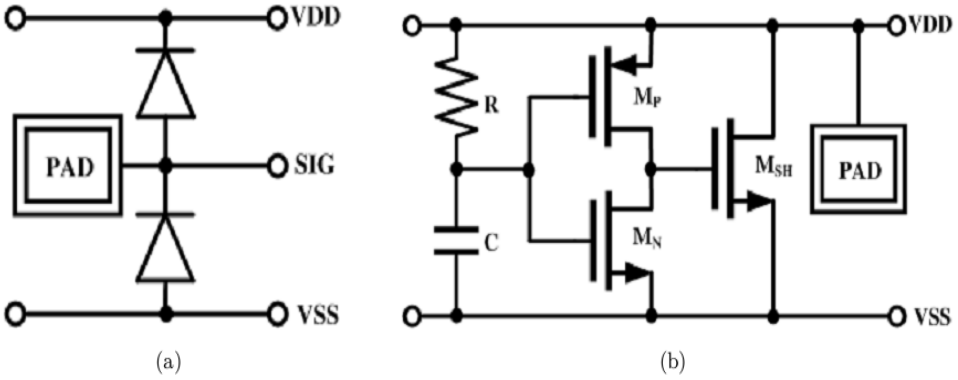


Figure 3.16: Pad structure with ESD diode protection

Momentary triggering of this MOS depends on RC time constant and the slew rate ESD voltage.

Layout Design: Layout of this front end receiver circuit is done in 1P9M2T0F1U (1-poly, 9-metal) stack with top metal of 2μm thickness. Spiral inductors and MIM (metal-insulator-metal) capacitors are laid on top metal layer for better Q-factor. All bias capacitors are realized by MOS capacitors. Width of various routing trace are optimized according to their utility like power, bias, signal etc. Maximum internally generated bias voltages which are more sensitive, are terminated in I/O pads to monitor as well as to override from external source, if required. In LNA layout the input is on the left, the output is on the right, and both are AC-coupled. Inductors are placed as far from each other as possible given the available area in order to reduce parasitic mutual coupling. In addition, signal routing is shieled with dummy layers the bias lines are shielded with ground and routed in such a way as to minimize the distances from them to the inductors. The layout diagram of LNA and front end receiver block with pad and ESD protection is shown in Fig 3.17 and Fig 3.18. A power-ground ring is made in the chip periphery to enable low resistance path from any pad to power and ground pads for better protection from ESD events. This ring is made using multiple metal layers in parallel to reduce resistance. A pad pitch (adjacent pad center to center distance) of 100μm is chosen for DC pads and 100μm for RF pads. Total area consumption of LNA chip is 1mm * 1.2mm and receiver occupies area is 2mm*1.2mm.

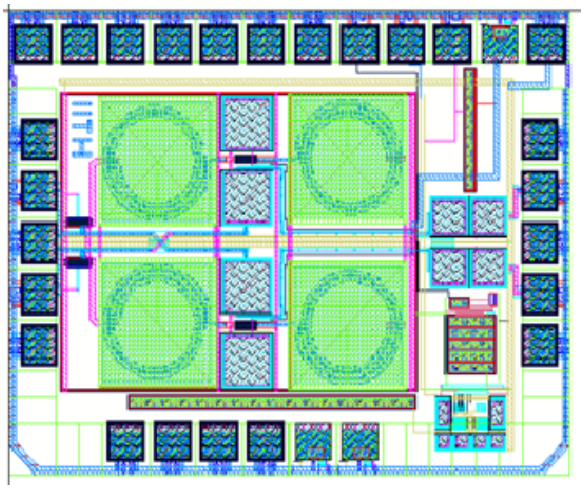


Figure 3.17: LNA layout

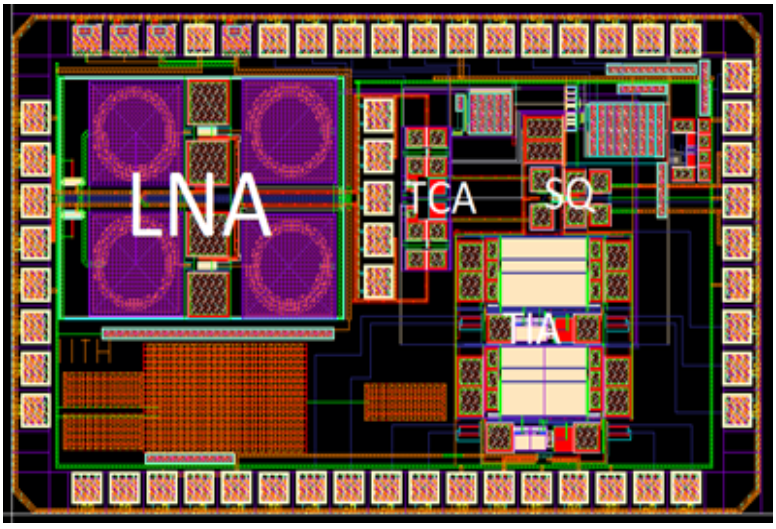


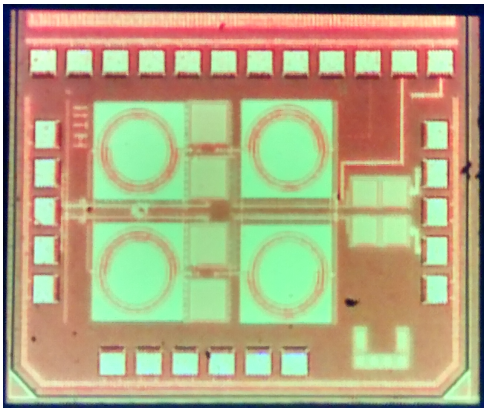
Figure 3.18: Post layout of main path Receiver

3.5.1 Experimental Results

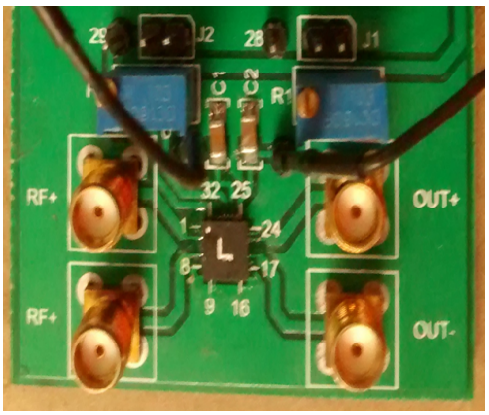
3.5.1.1 Measurement Results of LNA

3.5.1.1.1 Measurement setup The circuit has been designed and fabricated in the UMC 65nm CMOS technology. The LNA die microphotograph is shown in Fig. 3.19(a) and board of LNA is shown in Fig. 3.19(b). Die characterisation is done using Cascade Mircotech semi-

automatic probe station, Summit 12000. DC pad's interface are enabled through tungsten tip of 7μm diameter. The probes used for RF measurement are $|Z|$ - probe which is a type of Air Coplanar Probe with G-S-G-S-G (ground-signal-ground-signal-ground) configuration. The probe pitch is 100μm (adjacent pin center to center distance). To force and sense multiple DC voltages, a 12-pin Multi-$|Z|$ probe with 100μm pitch is used. Control of different bias and supply voltages are managed through tiny switches mounted in PCB.



(a) Chip microphotograph



(b) Assembled board of LNA

Figure 3.19: Chip microphotograph and assembled board of LNA

The noise measurements were done using a noise figure meter in spectrum analyzer. Since the measurement cable is lossy, the measured noise figure number must be subtracted by the input cable attenuation as well balun loss. The measurement setup is shown in Fig. 3.20.

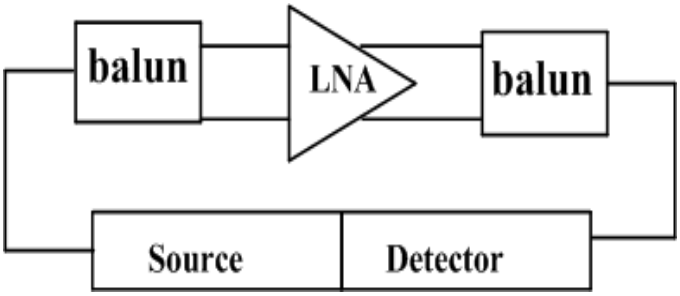


Figure 3.20: Measurement set of Noise Figure

If the loss at the output is small, the LNA noise figure can be estimated as follows

$$NF_{LNA}(dB) = NF_{measured}(dB) - L_{cable}(dB) - balun_{loss}(dB) \tag{3.44}$$

Where Lcable is the input cable loss.

Agilent table-top power supplies are used for DC testing and bias current measurement. The S-parameters are measured using Agilent Vector Network Analyser (VNA), E8361A. Agilent noise figure analyzer, N8975A along with Agilent noise source is used for noise measurement. RF measurement set-up including probe tips is calibrated using Cascade Microtech CSR-8 calibration substrate on SOLT standard. All measurements are done at room temperature. Using same instrument board also tested.

3.5.1.1.2 Result and Discussion Fig. 3.22 shows the measured (packaged die) and simulated S-parameters. LNA charaterization is done by both ways on-wafer as well board (packaged die), only packaged results are mentioned below. Differential LNA characterization is done using 4 port network analyzer with true (balance) mode. S parameters of LNA almost matching with simulation result over a bandwidth of 0.3-3GHz. Fig. 3.21 shown S parameter of packaged die taken from Vector network analyzer. Further all S parameters are compared with simulation

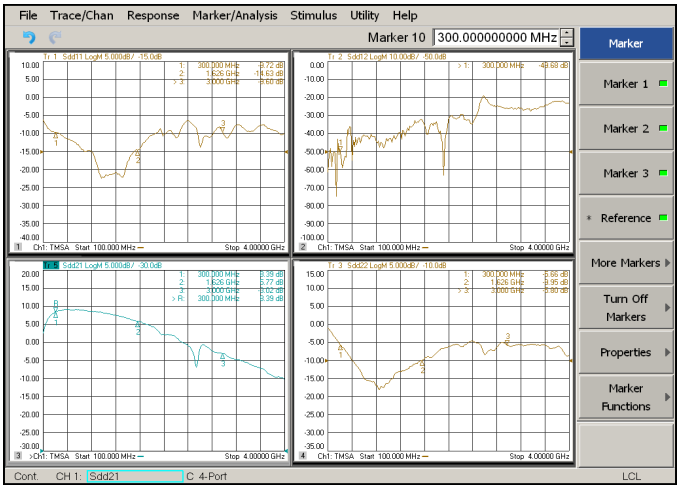


Figure 3.21: Measured S parameter of LNA with buffer from Network Analyzer

results in Fig. 3.22. Fig. 3.22(a) shows the S11 plots from simulation and measurements in the same graph for Id=12.5 mA. They are slightly off-tuned, nonetheless the plots share the same

trend. Since the matching is dominated by the passive elements at the input, the discrepancies most likely come from parasitic components associated with the inaccuracy of the layout modeling and simulations. Package die result is falling around 2GHz because board paracitics are dominating. Maximum measured S_{21} is 12.1dB and minimum is 9dB over the bandwidth. Accounting for the source follower buffer loss of ≈ 8-9 dB, the total simulation voltage gain is 20 dB. Measured S_{12} is below -20 dB and S_{22} is almost below -10 dB over the frequency range.

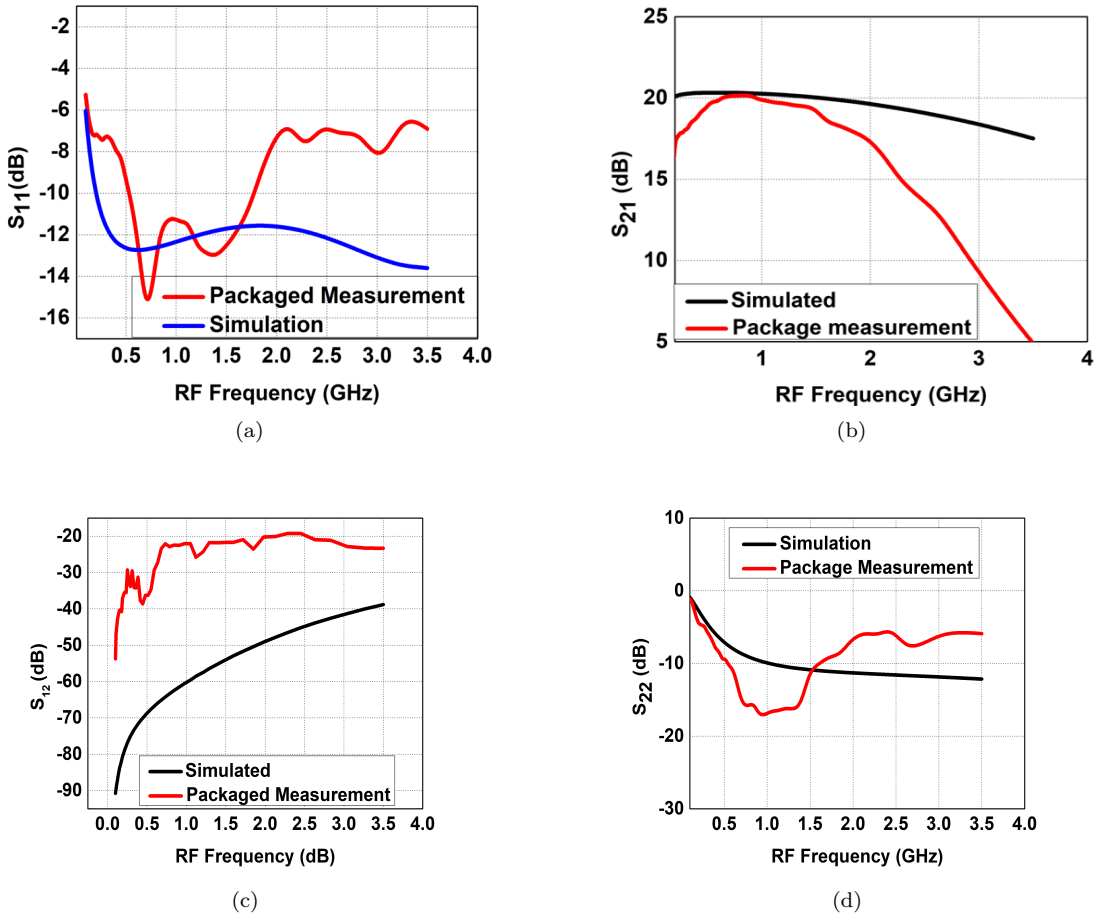


Figure 3.22: Measured S parameter of LNA without buffer

S_{22} does not depend on the bias current and only weakly depends on the frequency. The measured S_{22} is better than -10 dB from 0.1 GHz to 3.5 GHz. The buffer current is fixed at 5mA for all the measurements, and this makes S_{22} almost independent of the main stage bias condition. According to the data, we can then assume that ≈ 9dB loss occurs at the buffer stage.

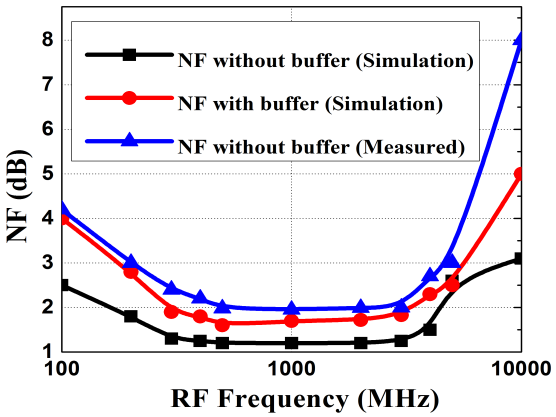


Figure 3.23: Measured Noise figure of LNA

For noise figure measurement off chip balun is used. In addition, The de-embedded noise figure measurement results are shown in Fig. 3.23 and comparison is drawn between the simulated and measured result. As shown in the plot, the minimum measured noise figure is approximately 1.7 dB at around 1.2 GHz and 12.5 mA bias current. For the same bias condition, noise figure is below 2 dB between 0.3 GHz and 3 GHz. It is expected that noise performance will get worse when bias current is reduced. The measured noise figure is around 0.2-0.5 dB higher than in the simulations. Since the induced gate noise is not included in the device model in simulations, it is likely a cause of discrepancies. This can be fixed by manually adding the gate-induced noise into the model.

The input 1dB−CP of the LNA was measured at 1.5GHz , which is around the mid band of the LNA. The measurement results are plotted for bias current 12.5mA in Fig. 3.24 . LNA linearity is measured for different bias current from 10mA to 16 mA.

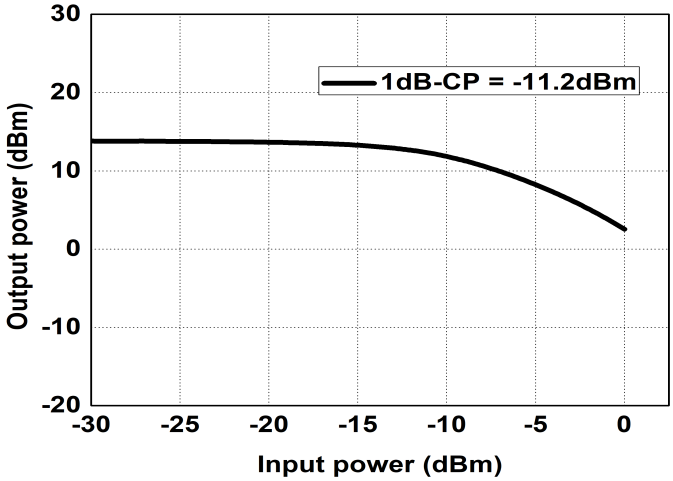


Figure 3.24: Measured 1dB-CP at 1.2GHz of LNA

Table 3.10: Measured Results and comparision of LNA

Ref.	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)	FoM	package
[34]JSSC 2017	0.1 - 2	17.5	<-10	2.9-3.5	10.6 - 14.3	2.2	21.34	180	16.5	On-wafer
[35]TCASII 2007	0.2 – 3.8	11.2	<-10	2.55-2.85	-2.7	1.2	1.9	65	14.2	NA
[36]ASSCC 2007	0.05 - 0.860	15	<-15	2.5	8.5	1.8	7.2	180	10.58	On-wafer
[37]JSSC 2011	0.002- 1.1	20	<-8	1.9	-1.5	1.8	18	90	13.8	MLP
	002- 2.3	21	<-8	1.7	-1.5	1.8	18	90	13.6	On-wafer
[38]MTTS 2011	0.7 - 2.7	17.3	<-8	2	5	1.8	17.1	180	14	On-wafer
This Work (Simulation)	0.3-3	20	<-10	1.2	0	1.5	18.75	65	14.9	
This Work (Measured)	0.3-2	17-20	<-10	1.3-1.5	-1.5	1.5	18.89	65	14	packaged

$$FoM = 20log(fRF) + CG - NF + IIP_3 + 10log(P_{DC}) \tag{3.45}$$

A Figure of Merit (FoM) given in (3.45) is suitable for evaluating the proposed LNA is given in Table 3.10 and the same is calculated for the related recent works as given in Table 3.10. Though [34] have better FoM, but it has more noise figure and area. Proposed architecture has more bandwidth at packaged level and low noise figure, so proposed architecture is the most suitable one for military application where noise is a major concern. Buffer loss has been de-embeded for all tabulated results listed in Table 3.10.

3.5.1.2 Measurement Results of Receiver

3.5.1.2.1 Measurement setup Chip microphotograph of main receiver is shown in Fig. 3.25. Measurements were done on a PCB as well module encapsulated chip-on-board. The board has differential RF inputs and differential fLO inputs. Off-board RF baluns (Markimicrowave 0010) were used to provide differential drives. At the output of the receiver, a differential buffer was added to isolate the loading effects seen in the mixer output stage. At IF output, balun (mini circuit) was added for a differential-to-single-ended conversion. These test boards were built with FR4 material. Fig. 3.26(a) shows a complete photograph of the assembled test board. Fig. 3.26(b) shows a complete photograph of the chip on board module. Agilent DC power supplies are used for DC characterisation. Agilent Vector Network Analyser (VNA), E8538 is used for LO signal generation and Rohde and Schwarz AMU200A base band signal generator is used for RF signal generation. Agilent noise figure analyser, N8975A is used for noise figure measurement.

The chip consumes total 63.5 mA current including all buffer and bias circuitry, while LNA consumes 12.5mA from 1.5V supply and mixer core consumes 20.1mA from 1.2V supply. The fLO signal needs to be 5 dBm at 1 GHz and 10 dBm at 3 GHz in order to maintain front-end functionality. These power levels are measured at the SMA connector inputs. The receiver works from .3G - 3GHz.

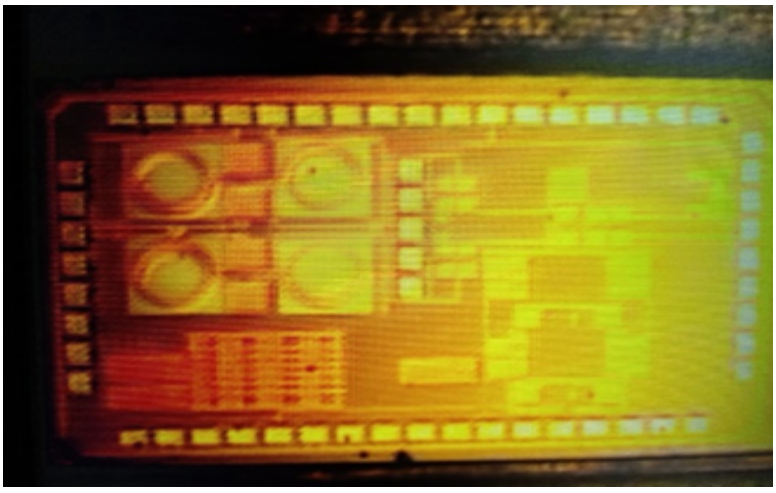
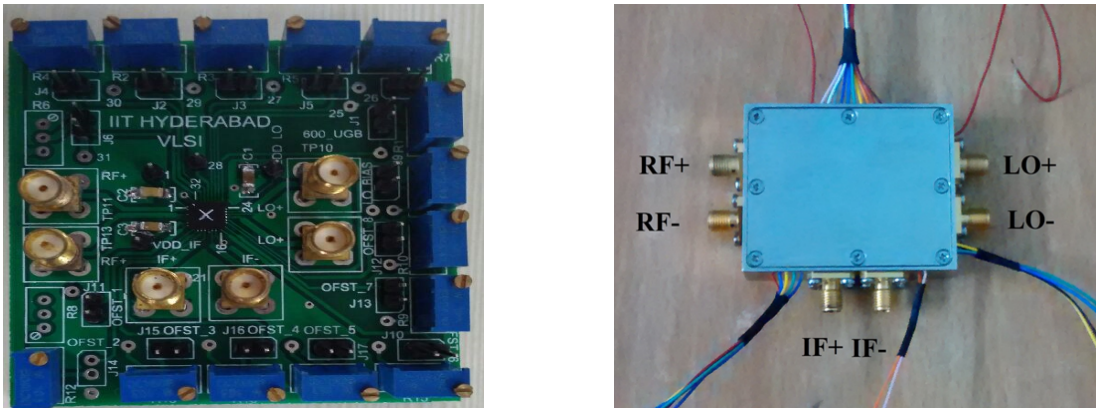


Figure 3.25: Microphotograph of main Receiver



(a) Assembled test board

(b) Chip on board of main Receiver

Figure 3.26: Test board and chip on board receiver

3.5.1.2.2 Result and discussion The input reflection S_{11} referring to a 50 Ω differential source impedance. The S_{11} measurement of receiver is done in similar way as done for LNA is shown in Fig. 3.27. S_{11} almost matches better than -10 dB. Minimum value of S_{11} is -9dBm. The S_{11} results include parasitics due to the connector and test boards.

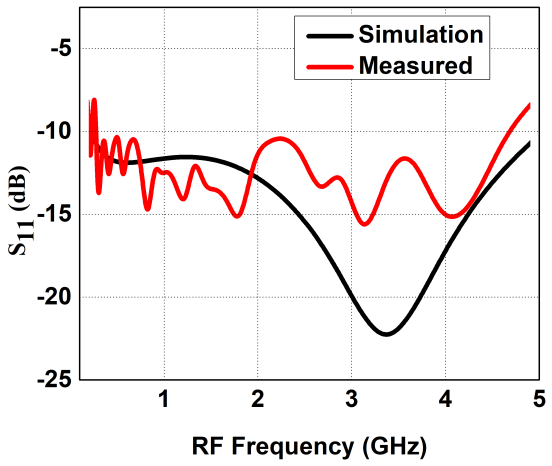
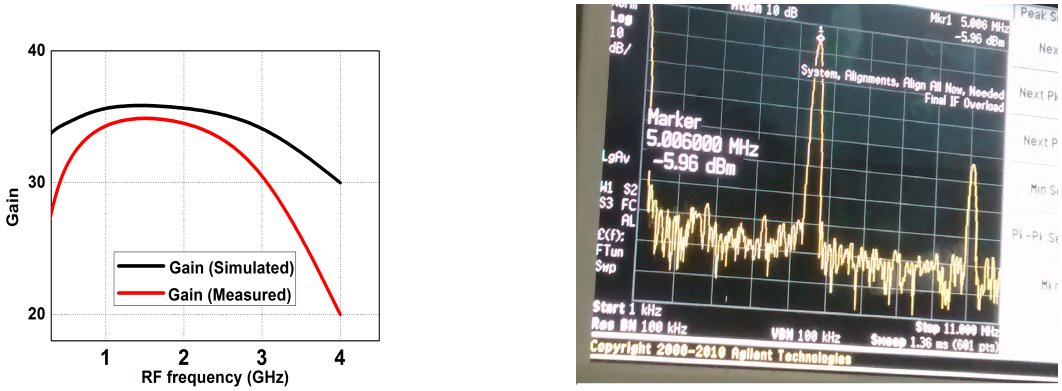


Figure 3.27: Measured input reflection of main Receiver

Fig. 3.28(a) shows conversion gain at a function of LO frequency for baseband frequencies of 5 MHz. The results include variations due to impedance mismatches at the LNA inputs. For an accurate measurement all the cables should have the same length and shorter cables are preferred

over long cables due to their lower losses. Chip on board and packaged dies board are having almost same performance. The difference between simulation and measurement is around 2dB is due to on chip paracitics. Cable and balun loss has de-embeded in measurement results. Thought it has common source amplifier as a buffer, but all results are excluded buffer. IF spectrum taken from spectrum analyzer is shown in Fig. 3.28(b) at 1G RF frequency @ -31dBm RF input power. It has approximately 8dB cable plus balun loss.



(a) Measured conversion gain of main Receiver

(b) IF spectrum of main Receiver

Figure 3.28: Spectrum of main receiver @ -31dBm RF input power

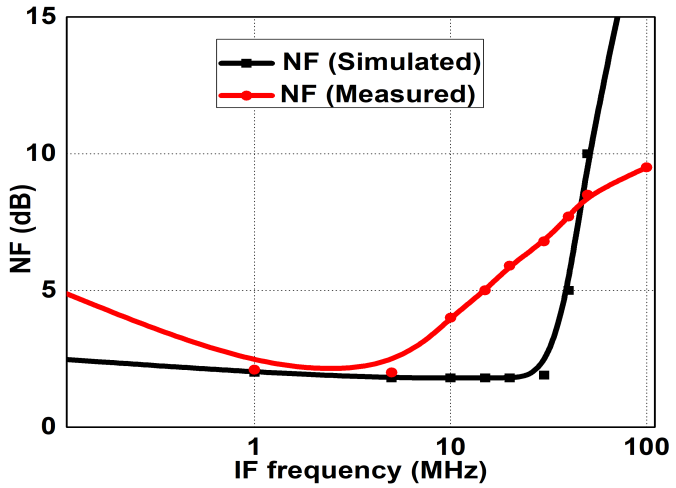


Figure 3.29: Measured noise figure of receiver

Noise was measured at various LO and RF frequencies using a noise figure meter. At 1.5 GHz fLO and 5 MHz baseband, the measured double-sideband noise figure (DSB NF) is 5.05

dB including all the balun, cable, board losses, and input mismatches. The estimated loss of the balun and cable (obtained from separate cable and balun measurements using a network analyzer) is 3.1 dB, and the de-embedded DSB NF is 5.05 dB − 3.1 dB = 1.95 dB. The 1.95 dB DSB NF still includes any board and SMA connector losses, since it is not possible to directly measure the loss on the PCB. Plot of de-embedded NF versus baseband for various RF bands are shown in Fig. 3.29. DSB NF is approximately 1.95 dB at 1.5 GHz RF and 5 MHz baseband.

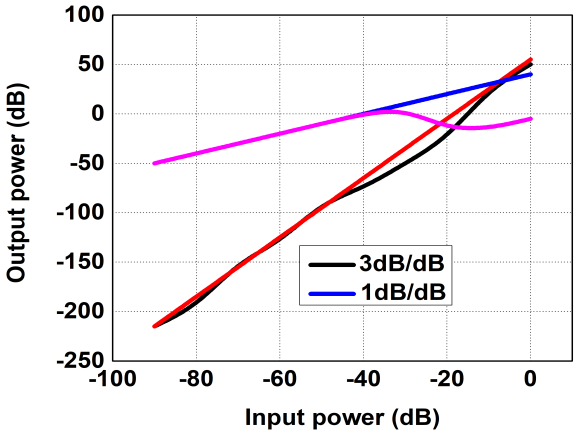


Figure 3.30: IIP_3 of main receiver

Fig. 3.30 the third-order intermodulation is shown at 1.5 GHz frequency, for instance. Two-tones are applied at 1.51 GHz and 1.525 GHz respectively, while LO is at 1.5 GHz frequency. The 1 dB difference between the two fundamental is shown in figure, is suspected from uncertainties of the off-chip wideband balun at LO port. Since the wideband off chip baluns are not very accurate through the whole range of frequency, the phase and amplitude imbalance at the output of the balun may cause distortion in the measurement. The distortion is negligible at the frequencies, where balun has the lowest phase and amplitude imbalance.

A Figure of Merit (FoM) given in (3.45) suitable for evaluating for the proposed High performance receiver is given in Table 3.11 the same is calculated for the related recent works as given in Table 3.11. Though [32] and [29] has better FoM but both has high noise figure. Thus the proposed architecture is the most suitable one for realization and overall figure of merit.

Table 3.11: Measured results and Comparison of main path Receiver

Ref.	FoM	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)
[1] JSSC 2015	18.23	0.1-2.8	50	<-10	1.8	+5(OB)	1.1	27-40	40
[32] ISSCC 2010	53	0.05-2.4	80		5.5	27	1.2/2.5	60	65
[29] VLSID 2016	29.22	0.4-4	36	<-15	3.5-7	2.5	1.2	38.4-55.2	65
[33] MTT 2012	17.3	0.6-3	42-28	<-8	3	-14	1.2	30	130
[53] ICICDT 2017	17.3	0.7-3	15-22	<-8	7.5-5.6	-3 - 9.2	1.2	22	130
This Work* Measured	22	0.3-3	37 @-31dBm	<-10	1.85	-6	1.2	44.5	65
This Work Simulation	29	0.3-3	41 @-47dBm	<-10	1.8	-5	1.2	44	65
*Sensitivity = -90dBm									

3.6 Summary

To summarise, this chapter a composite transistor pair is analyzed in detail. Further inductive degeneration is used to improve input matching and gain bandwidth. LVT/RVT MOS is compared and analyzed noise figure in both cases. Further input matching, noise figure, transfer function discussed in detail. To prove this concept LNA is designed and taped out. All measurement results are compared. Further a passive down conversion mixer is designed for better flicker noise and better linearity. LNA and downconversion mixer is integrated in single die. Integration issues are taken care. All performance parameters are measured and compared.

Chapter 4

Auxiliary Path Ultra Low Power Out of Band Sensing Subthreshold Receiver

4.1 Introduction

A CMOS transistor in strong inversion has square-law characteristics, a subthreshold CMOS transistor exhibits exponential characteristics similar to that of a bipolar transistor. Though extensively used in low-power analog circuits, subthreshold biasing has not been adequately explored at RF frequencies. The potential of implementing low-power RF circuits in subthreshold CMOS is investigated in this chapter. A review of performance of recently reported low noise wide band receiver using different techniques (subthredhold, saturation, etc) are listed in Table 4.1

.

Table 4.1: Review of recent ultra low power wideband receiver

Ref.	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)	Region of operation
[54]	0.17/0.433 0.915/0.868 /0.950/ISM	39	<-10	6.5	-8	1.8	5.08	180	Saturation
[55]	2545-2700	8.89	<-19	8.85	-9.5	1.2	3.12	180	Saturation
[56]	0.433/0.860 0.915/0.960	50±2	<-10	8.1±0.6	1.15±0.05	0.5	1.15±0.05	65	Low VDD
[57]	0.85-2.55	55	<-8	13.6	-7.5	0.8	0.53-0.97	28	Low VDD
[58]	0.902-0.928	17.7		6.7	-7.5	1	0.218	90	Subthreshold

4.1.1 Subthreshold MOS Operation

Subthreshold biasing is a standard circuit design technique used extensively in CMOS analog circuits to decrease power consumption [59]- [60]. The main advantage of biasing a CMOS transistor in the subthreshold region is the significant increase in the transconductance to bias current ratio (gm/I_D) when compared to the operation in strong inversion. Recently, subthreshold operation has been exploited in ultra low power digital circuits [61] - [62] by lowering the supply voltage below the threshold voltage of the transistors. The drain current, i_D, of an NMOS transistor operating in weak inversion can be approximated by the following equation [59]:

$$i_D = \frac{W}{L} * I_{D0} exp \frac{v_{GS}}{n(KT/q)} \tag{4.1}$$

where n is the subthreshold slope factor, (I_{D0}) is a process-dependent parameter, k is the Boltzmann's constant, T is the temperature (K), and q is the charge of an electron. Thus, the device characteristics change from square-law in saturation to exponential in sub threshold. The gate-source voltage below which the transistor can be assumed to operate in subthreshold region is given approximately by:

$$v_{gs,subthreshold} = v_t + n\frac{KT}{q} \tag{4.2}$$

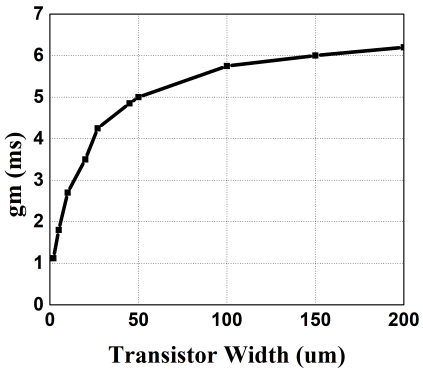
In subthreshold region, the drain current becomes relatively constant if V_{DS} is raised above 3kT/q ($\approx 78mV$). The transconductance (gm) of a transistor in strong inversion is given by:

$$g_{(m,strong,inversion)} = \sqrt{2I_D\mu_n C_{ox} * W/L} \tag{4.3}$$

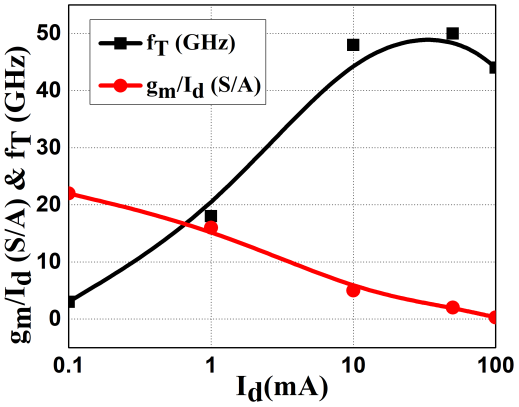
where μ_n is the electron mobility and Cox is the oxide capacitance per unit area. The subthreshold transconductance, on the other hand, is independent of the aspect ratio and is given by:

$$g_{m,threshold} = \frac{I_D}{nKT/q} \tag{4.4}$$

Fig. 4.1(a) shows the g_m of a 0.18 μm NMOS transistor when the transistor width is increased from 2.5 μm to 200 μm, with a constant bias current of 300 μA. The increase in gm is significant as the device width is increased and one moves from the strong inversion region following (4.1), to subthreshold region where (4.4) is valid as shown in Fig. 4.2. Subthreshold circuits also require lower voltage headroom, leading to easier stacking of blocks or lowering of supply voltage. The voltage swing required is also lower than that in typical CMOS circuits: for instance, a differential pair requires only about 78mV (3kT/q) for hard switching.



(a) Transconductance of an NMOS transistor with 0.18 μm length (L) and a bias current of 300 μA.



(b) Plot of f_T and gm/ID of a 120 μm / 0.18 μm NMOS transistor.

Figure 4.1: Transconductance and f_T plot of NMOS transistor

Frequency Potential of Subthreshold Circuits in Deep Sub-micron CMOS:

Technology scaling has made possible CMOS circuits operating at 100 GHz and beyond [63]. However, in subthreshold f_T has improved with technology scaling. A deep sub-micron MOS device operating in weak inversion region can provide sufficient transconductance for many low

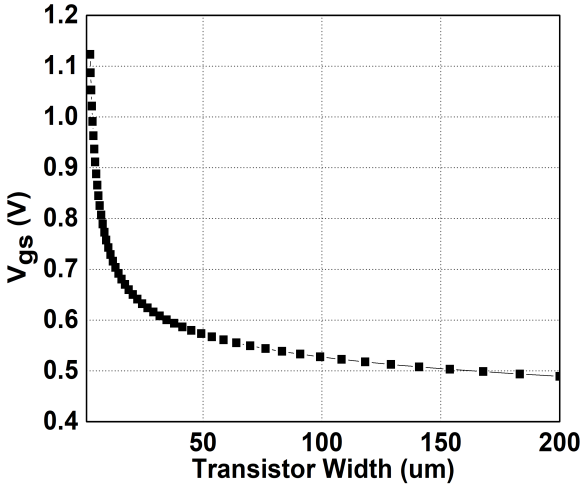


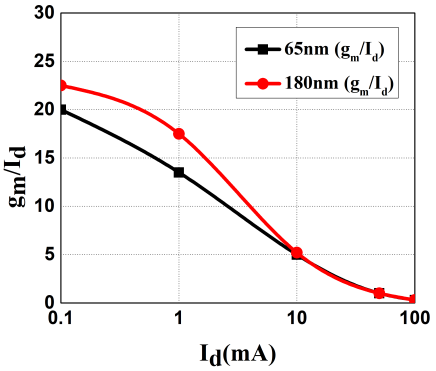
Figure 4.2: Width vs V_{gs} NMOS transistor with 0.18 μm length (L) and a bias current of 300μA.

power RF applications when used with suitable passive networks.Though the gm/ID ratio is higher than that in strong inversion, the absolute value of transconductance is significantly lower. As can be seen from (4.4), increasing W/L without changing ID does not increase transconductance, unlike in strong inversion. However, if the current density is kept constant, gm increases linearly with W/L. Hence, one can achieve the same transconductance for lower current by using a larger active device in the subthreshold region, resulting in extremely low-power consumption. On chip inductors can then be used to resonate out the higher capacitances associated with the larger transistor. The higher output resistance of a subthreshold transistor can also help increase its voltage gain. The transition frequency, f_T, is defined as the frequency at which the magnitude of the short-circuit common-source current gain falls to unity. The transition frequency of a subthreshold CMOS transistor is also much lower than that of a CMOS transistor in strong inversion and is given by:

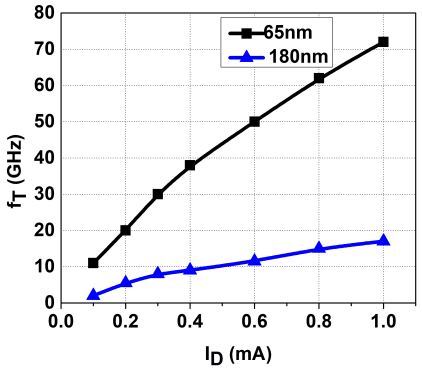
$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{4.5}$$

The simulated f_T, and gm/Id are plotted in Fig. 4.1(b) against the drain current I_D for a 120 μm / 0.18 μm NMOS transistor in a 0.18 μm process. The peak f_T of the device is near to 50 GHz at a bias current of 30mA. The gm/Id ratio at this bias point is only 2.07. This ratio is about an order of magnitude higher in the subthreshold region, where f_T is below 10 GHz. Technology

scaling will further increase subthreshold f_T, making it possible to operate weak inversion devices in higher frequency bands like 5 GHz too. Fig. 4.3(a) shows the simulated transconductance to bias current ratio of NMOS transistors in 180 nm and 65 nm CMOS processes. The simulated subthreshold transition frequencies of these devices are plotted in Fig. 4.3(b). All the transistors are minimum length devices. However, the W/L ratios for all the devices are kept approximately equal. The drain-source voltages used are the rated supply voltages for these processes.



(a) Transconductance to bias current ratio (gm/ID) in subthreshold and strong inversion regions across process technology nodes.



(b) Transition frequency of subthreshold NMOS transistors across process technology nodes.

Figure 4.3: gm/ID and f_T plot of subthrehold MOS

As seen in Fig. 4.3(a), gm/ID increases by about an order of magnitude from strong inversion to weak inversion in all the process nodes. At a bias current of 600 μA, the subthreshold f_T of the 65 nm device is above 50 GHz, as shown in Fig. 4.3(b). This is as high as the peak f_T of the 180 nm device in strong inversion shown in Fig. 4.1(b).

Although, 65nm node provides far higher f_T than 180 nm device in week inversion shown in Fig 4.3(b). However, 65nm process is 3-4 times costly than 180nm, since it is a auxiliary receiver for sensing out of band signal, so design has been carried out in 180nm. Further observed that the f_T of the 180 nm device in subthresold region are less than 10GHz. The better gm/ID ratio in subthreshold potentially exploited to reduce the power consumption of wireless receivers in low-power applications. Therefore, the design a wideband subthreshold receiver is a challenging task. The design architecture of subthreshold receiver is given in below sections.

4.1.2 Power Consumption in Wireless Front-ends

Lowering the total power consumption in battery powered wireless communication devices is critical so as to avoid frequent battery recharge or replacement. The total power consumption in a front-end is dependent on a multitude of factors. The sensitivity specification of the front-end determines the minimum gain and maximum noise figure of the receiver, both of which are dependent on the power consumption in receiver circuits. The output power requirement of the power amplifier is also extremely important in determining the total power consumption in typical wireless front-ends. The carrier frequency and process technology also affect the total power consumption. For example, if high Q passives are available at the operating frequency in the process technology selected, power consumption in amplifiers and oscillators can lowered significantly without compromising gain and noise performance. However, such passives are not available in low-cost CMOS processes. The power consumption in a wireless device is also dependent on the bandwidth and the supported data rate. Higher bandwidth and data rate generally requires higher transconductance in analog circuits and higher clock speeds in digital circuits, respectively, both of which increase power consumption. Complex modulation schemes requiring high processing power in the digital baseband section can also increase the total power consumption. Another important factor in determining the total power consumption in front-ends is the blocker profile of the standard. If the receiver has to work in the presence of strong interferers close to the signal spectrum, the linearity and phase noise specifications become more stringent, potentially leading to significant increase in power consumption in the front-end circuits.

4.2 Subthreshold Low Noise Amplifier

As explained before, subthreshold CMOS transistors in deep sub-micron technologies can be utilized to develop extremely low-power RF circuits. However, subthreshold biasing of RF circuits has not been adequately explored in the past. A subthreshold LNA is designed for 2-5 GHz in 0.18 μm CMOS process to demonstrate micro-power RF circuit implementation using weak inversion devices.

4.2.1 Design and Implementation Subthreshold LNA

As analog and radio frequency (RF) circuits operating in subthreshold regime exhibit higher thermal noise, lower bandwidth, and poor linearity, the design of wideband LNA becomes extremely challenging in-spite of the fact that subthreshold biasing provides higher gm/ID compared to strong inversion. Fig. 4.4 shows the implemented LNA [64] that achieves moderate noise figure (NF), wide bandwidth, good linearity, and moderate gain while being biased in subthreshold regime and achieving excellent energy efficiency. The LNA incorporates a common gate (CG) stage followed by a CS-CG stage with current reused, gain-boosted, and feed-forward noise cancellation. The CG stage load is resistive (R_{d1}). The CS-CG stage load, L_{d3} provides shunt peaking by resonating with the total capacitance at drain of M3, thus providing bandwidth extension. The resistance R_{d3} is added in series with L_{d3} to not only reduce the quality factor of the inductor, so that the peak at resonance is controlled, but also to enhance the low frequency gain.

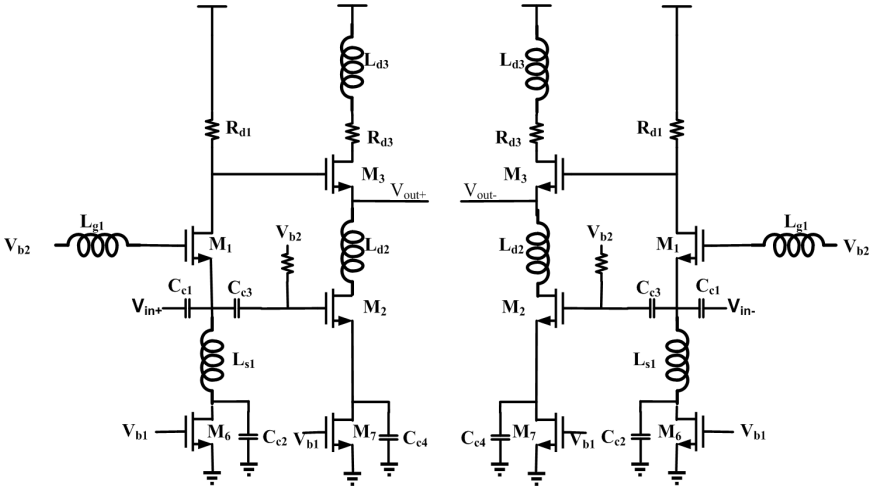


Figure 4.4: Low Noise Amplifier for subthreshold receiver

4.2.1.1 Wideband Input Matching, Gain and Noise Analysis:

Input matching in a wideband CG-LNA is accomplished by making its transconductance, gm=1/RS, where RS = 50Ω is the source impedance. Achieving this transconductance in subthreshold regime would require a large device resulting in a large input capacitance (Cgs), which in turn

would reduce the bandwidth. However, by introducing an inductor (Lg1) at the gate of the input device, the input matching dependency on gm is minimized. The gate inductor modifies the gm and reduces the effect of Cgs, so that the frequency, at which Cgs dominates, is moved to higher value.

Wideband LNA incorporates a CG-stage followed by a CS-CG current-reused gain-boosting stage. Thus the gain analysis can be done by decoupling the two stages and analyzing the gain of each stage independently and then obtaining the overall gain. Similarly noise from each component is described in detail in [64].

4.3 Active Gilbert Cell Down Conversion mixer

The schematic of proposed wide band low power active mixer biased is shown in Fig. 4.5. The transconductance MOS are biased in subthreshold region to attain very low power consumption. The mixer core (LO pair transistor) consists of the four switching transistors and RF pair consists two transistor. RF pair is biased lower than the threshold voltage. The Gilbert cell employs emitter degeneration R and C for the transconductance stage [65]. Resistive and capacitive degeneration in the transconductance stage allows a signicant extension of the RF bandwidth [66]. This is, however, at the expense of reduced conversion gain because, effective transconductance will get reduced as given in 4.6.

$$g_{m,eff} = \frac{g_m}{1 + g_m(R_{deg}||C_{deg})} \tag{4.6}$$

To overcome the gain degradation due to the degeneration, capacitive cross coupling [67] is introduced in RF pair. This will effectively increase the transconductance of the RF stage, so that the overall gain of down conversion mixer is increased. One issue, is that the crosscoupled capacitance is required to be much larger than the parasitic capacitance between the gate and the source for the transistor. Otherwise, it could degrade the noise factor and input matching. In order to analyze the conversion gain of the proposed structure we need to use the principle of superposition as shown in Fig. 4.7(a), Fig. 4.7(b). Common gate amplifier shown in Fig. 4.7(a) A_{V1} can be written as

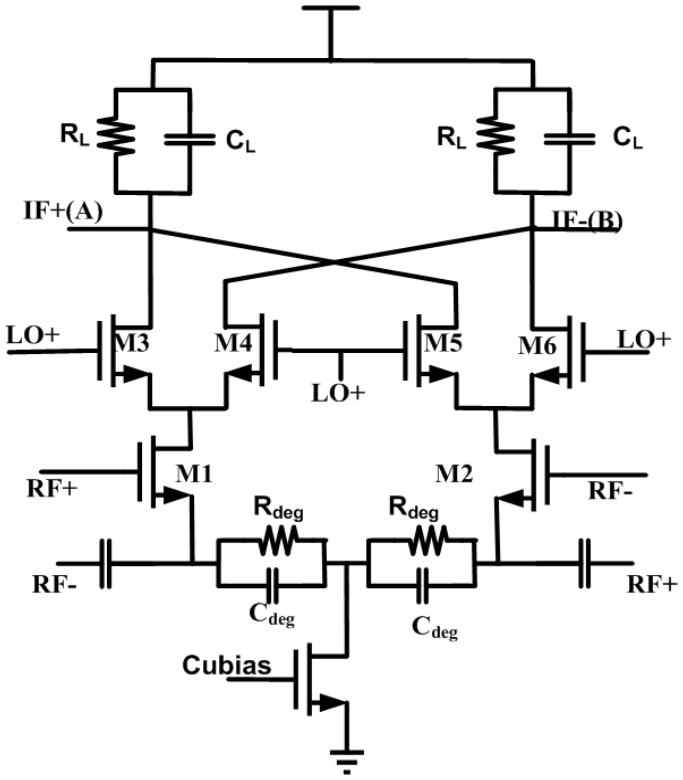


Figure 4.5: Proposed Gilbert Cell (Active Gilbert cell Down conversion Mixer with bandwidth Extension) for subthreshold receiver

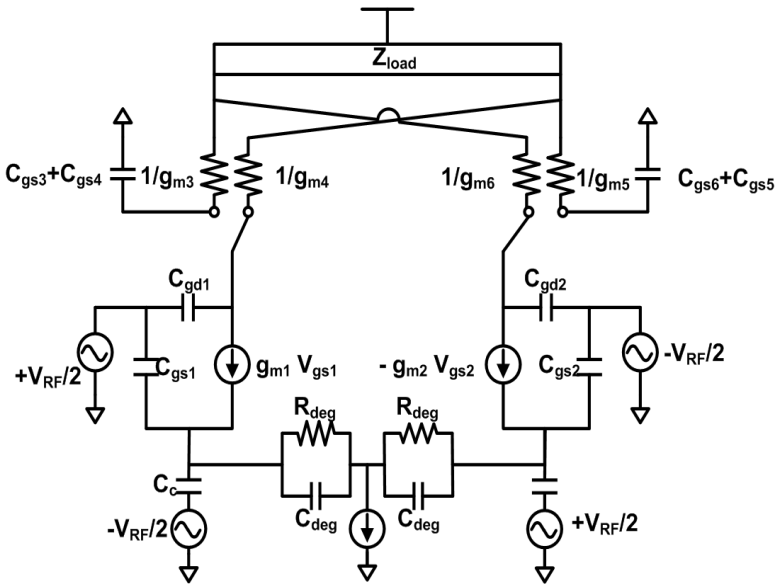
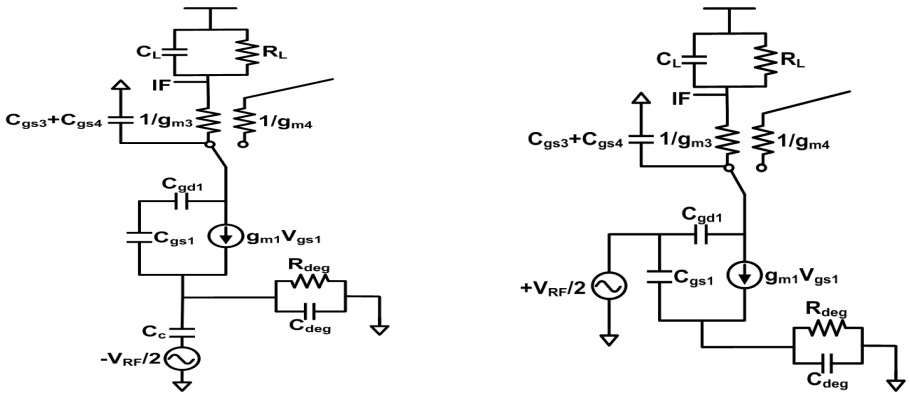


Figure 4.6: Small signal model of proposed gilbert cell



(a) Common gate Amplifier. (b) Common source Amplifier.

Figure 4.7: Superposition theorem in CCC in input pair of mixer

$$A_{V1} = -\frac{g_m}{1 + g_m(R_{deg}||C_{deg})} * R_L||C_L||\frac{1}{g_{m3}} \tag{4.7}$$

Similarly for common source amplifier in Fig. 4.7(b)

$$A_{V2} = -\frac{g_m}{1 + g_m(R_{deg}||C_{deg})} * R_L||C_L||\frac{1}{g_{m3}} \tag{4.8}$$

Total conversion gain of down conversion mixer can be written as

$$A_V = A_{V1} + A_{V2} = \frac{2}{\Pi} * 2 * \frac{g_m}{1 + g_m(R_{deg}||C_{deg})} * R_L||C_L||\frac{1}{g_{m3}} \approx \frac{2}{\Pi} * g_{m,eff} * (R_L||C_L) \tag{4.9}$$

Common gate input stage with CCC (capacitive cross coupling) leads to two fold increase in effective transconductance which in turn doubles the gain. Thus, the current consumption is reduced. Finally, it is also interesting to note that the capacitive cross-coupling does not add much cost and complexity.

4.3.1 Transfer Function of Active Gilbert Cell Down Conversion Mixer

To analyze transfer function small signal circuit is drawn as shown in Fig. 4.6. A peaking capacitor provides a zero in the transfer function, which extends the transconductance stage bandwidth with relaxed resistive source degeneration, as shown by the following expression and Fig. 4.8. Small signal analysis results in differential transfer function

$$A_{v(s)} = \frac{(V_{op} - V_{on})}{(V_{in} - V_{ip})} = \frac{-(A_v(1 + \frac{s}{z_1}))}{((1 + \frac{s}{p_1})(1 + \frac{s}{p_2}))} \tag{4.10}$$

$$z_1 = \frac{1}{(R_{deg}C_{deg})} \tag{4.11}$$

$$p_1 = \frac{1}{(R_L||\frac{1}{g_{m3}}) * C_L} \tag{4.12}$$

$$p_2 = \frac{1}{(C_{deg} + C_c + C_{gs})(1/g_m||R_{deg})} \tag{4.13}$$

WhereA_v is the conversion gain, p1 and p2 are the poles at output and input, z1 is the zero due to RC degeneration.

By introducing zero in a transfer function, it adds $+20dB$ and cancel the pole as a result it enhance high frequency response of the circuit, as from (4.11), it increase high frequency performance of circuit. So by introducing zero in active gilbert cell mixer bandwidth is improved.

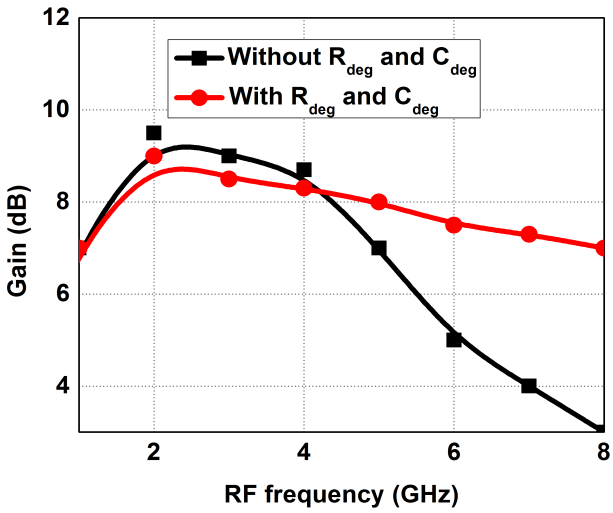


Figure 4.8: Bandwidth extension using capacitive degeneration

4.3.2 Noise in Current-Commutating Mixers

Refer to the CMOS Gilbert cell mixer in Fig. 4.5, there are different noise sources in this mixer shown in Fig 4.9

1. Noise from load $R_L||C_L$ (noise current $= i^2_{(n,R_L)} = 4kT/(R_L||C_L)$)
2. Noise from RF transconductors (MN1-MN2) ($i^2_{M1,M2} = 4kT\gamma g_m$)
3. Noise from switching pairs (MN3-MN4 and MN5-MN6)($i^2_{M3-M6} = \frac{K}{C_{OX}} L^2 * \frac{1}{f} * I_D$) (can be neglected)
4. Noise from R_{deg} resistor ($i^2_{(n,R_{deg})} = (4kT/R_{deg})$)
5. Due to input source resistance ($i^2_s = v^2_s * g^2_m$)

Noise Figure = NF = $\frac{\text{total noise}}{\text{noise of noise cource}}$

Noise figure for bandwidth enhanced double balance gilbert cell architecture is expressed below

$$NF = \frac{\Pi^2}{4}(1 + \frac{\gamma g_{m,eff}}{g^2_{m,eff} * R_s} + \frac{1}{(R_L||C_L) * g^2_{m,eff} * R_s} + \frac{1}{R_{deg} * g^2_{m,eff} * R_s}) \tag{4.14}$$

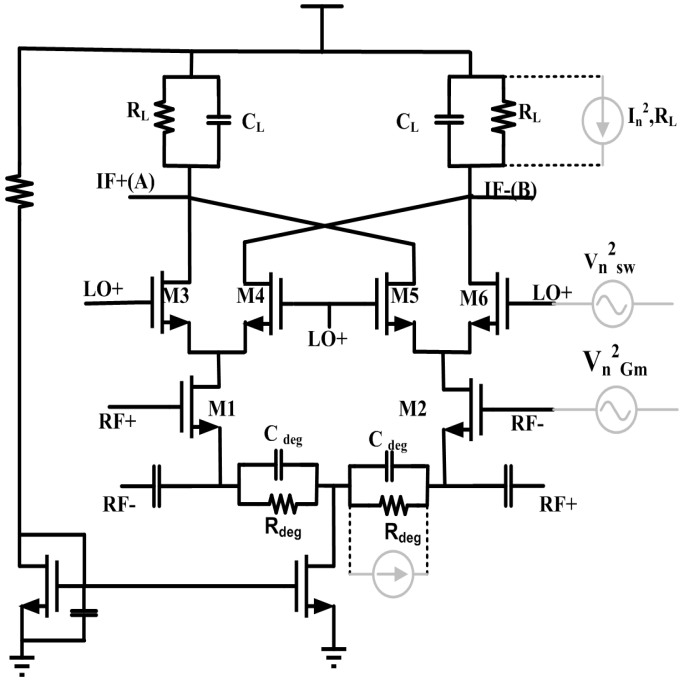


Figure 4.9: Noise sources in Proposed Down Conversion Mixer.

As compare to the conventional gilbert cell mixer, degeneration introduces additional fourth term as given in (4.14). While an extra term might introduce slight noise, this gets balanced by the improvement in conversion gain due to CCC technique.

4.3.3 Non-idealities of the Mixer

Linearity is an important measure of a single block or the whole receiver. The receiver must be able to receive a weak signal in the presence of strong interferes. There are several measures of linearity. The most commonly used receiver linearity tests are input 1-dB compression point (ICP or P1dB) and the third-order intercept point (IP3). In addition, the second-order intercept point (IP2) is a figure-of-merit for certain receiver architectures, such as DCRs. Linearity tests are typically performed with single-tone or two-tone sinusoidal signals.

4.3.3.1 Intermodulation Distortion

The third-order nonlinearity of Gilbert cell MOS mixers is primarily determined by the intrinsic device nonlinearity of RF transconductor. This is particularly true when switching pairs respond to quasi-square-wave LO and the harmonic distortion in transconductor is nonetheless dominant. Approaches to improve intrinsic MOSFET linearity include adjusting device DC operating point and increasing gate overdrive voltage V_{ov}. It is apparent that as gate overdrive increases the inherent linearity of NMOS improves as well [68]. In presence of peripheral circuit components, the resulted IIP_3 will no doubt be degraded.

The second-order linearity of mixer is more interesting to study. One significant mechanism comes from the self-mixing, which is resulted from capacitive coupling (finite isolation) between RF and LO ports. Besides self-mixing, both RF transconductor and switching pairs introduce even order nonlinearity. Mismatch and imbalance in switching pair fundamentally limit the maximum attainable second-order linearity. At device level, the mismatch includes threshold voltage V_{TH}, process-dependent constant $\mu\ C_{ox}$, and temperature, doping gradient induced device dimension difference. At signal level, the mismatch refers to LO duty cycle imbalance, and parasitic capacitance loading effects.

4.3.3.2 Integration issues

Several issues have to be accounted during integration, the main one being DC isolation from one stage to another. For this purpose large on-chip capacitors are used between every stage except for the output buffer which takes its bias from the previous mixer stage. The balun is multi-purpose and used both in the output of the LNA and also to convert the single ended frequency to differential owing to the fact that the LO port of the mixer needs to be differential in operation. Off chip broad band balun is used. It can handle broad band signals at low impedance levels while being completely differential in operation. The source follower buffer is used for the IF port matching. An attempt was made to minimize as many different bias sources as possible through the use of resistive dividers and blocking capacitors that efficiently channel bias to the needed points. Inductor optimization was crucial during integration stage as the

inductor spacing was kept at an optimal distance to avoid unwanted negative mutual coupling between two adjacent inductors.

4.4 Fabricated Fully Subthreshold Receiver

The subthreshold receiver circuit blocks diagram LNA and gilbert cell mixer discussed in the previous section is designed simulated and integrated as shown in Fig. 4.10, for the proof of concept and feasibility. The same is optimized here for fabrication, accounting for parasitics. In this section, design, fabrication, characterization and measurement results of a fully subthreshold receiver have been discussed.

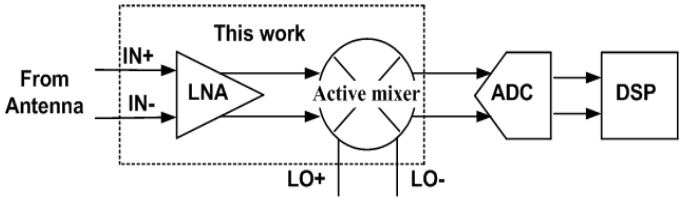


Figure 4.10: Block diagram of Subthreshold receiver

Full Circuit description

This receiver circuit is designed using UMC 180nm RF CMOS technology in Cadence design environment and simulated with SpectreRF simulator. Physical verification is done in Mentor Graphics Calibre tools. Fully differential LNA and gilbert cell down conversion mixer is integrated, integration issues has been taken care. A source follower buffer is designed and added at the output for output matching and measurement purpose. High overdrive voltage is provided for its current source to reduce capacitance at the output node. All stages including buffer are designed for 1.8V supply voltage. Buffer consumes $\approx$ 6mA current and adds loss of $\approx$ 8dB. All device dimension of Fig. 4.5 are listed in Table 4.3

Table 4.2: Circuit element values and transistor aspect ratio for the implemented subthreshold LNA

$(\frac{W}{L})_1$	$(\frac{W}{L})_2$	$(\frac{W}{L})_3$	$(\frac{W}{L})_6$	$(\frac{W}{L})_7$	
$(\frac{150um}{180nm})$	$(\frac{170um}{180nm})$	$(\frac{25um}{180nm})$	$(\frac{95um}{180nm})$	$(\frac{105um}{180nm})$	
L_{g1},L_{d2}	L_{s1}	L_{d3}	R_{d1}	R_{d3}	R_1
$3nH$	$5.5nH$	8nH	700Ω	200Ω	1.2KΩ
C_{C1}=C_{C2}=C_{C3}=C_{C4}=C_{C5}=5pF					

Table 4.3: Circuit element values and transistor aspect ratio for the implemented subthreshold Mixer

$(\frac{W}{L})_{M1-M2}$	$(\frac{W}{L})_{M2-M6}$	R_L	C_L	R_{deg}	C_{deg}
$(\frac{105um}{180um})$	$(\frac{75um}{180um})$	$2K\Omega$	1pF	500Ω	1pF

Bias circuit

All bias voltages are generated internally to counter the process variation. Replica biasing technique is used for generating all bias voltages. Design is optimized to avoid the need of multiple bias voltages of small differences and to use similar bias voltages at multiple MOS devices. The circuit employed for complete bias generation is shown in Fig. 4.11.

Four bias voltages are derived in total. A 550 mV (Cubias) for biasing tail current source MOS and 900 mV (RFbias) for both subthreshold stage transconductance MOS. Bias voltage for switching MOS is chosen as 1.1 mV (LObias) and 600mV(SFbias) for buffer bias. Complete bias circuit consumes 270μA current from 1.8V supply voltage.

Layout Design

Layout of this ultra low power receiver circuit is done in 1P6M (1-poly, 6-metal) stack with top metal of 2μm thickness. Spiral inductors and MIM (metal-insulator-metal) capacitors are laid

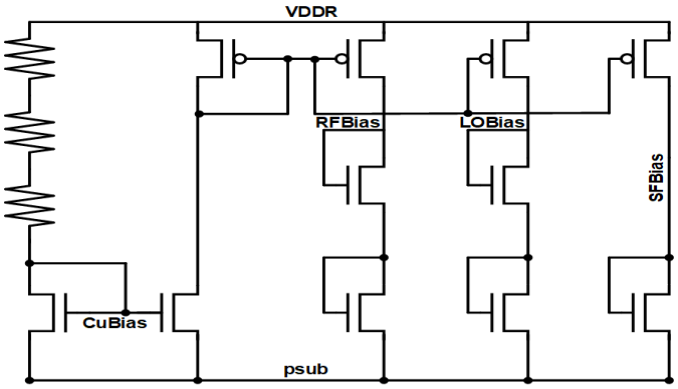


Figure 4.11: Schematic diagram of bias generation circuit

on top metal layer for better Q-factor. 6μm trace width is chosen for all inductors for better area efficiency. All bypass capacitors are realised by MOS capacitors. Width of various routing trace are optimized according to their utility like power, bias, signal etc. All internally generated bias voltages are terminated in I/O pads to monitor as well as to override from external source, if required. A power-ground ring is made in the chip periphery to enable low resistance path from

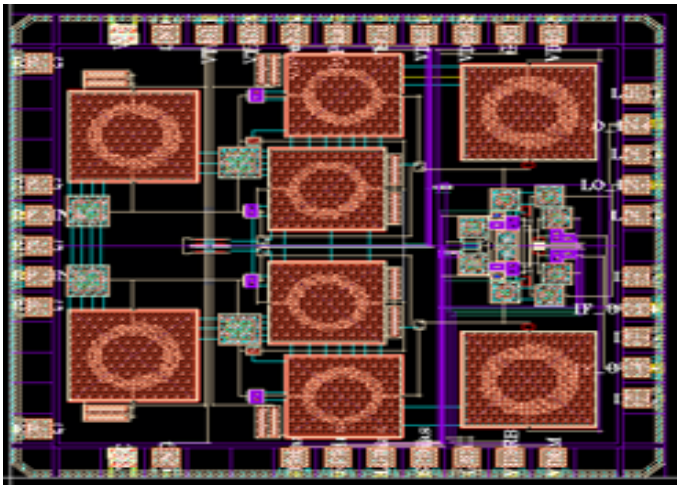


Figure 4.12: Complete layout diagram of subthreshold receiver

any pad to power and ground pads for better protection from ESD events. This ring is made using multiple metal layers in parallel to reduce resistance. A pad pitch (adjacent pad center to center distance) of 100μm is chosen for DC pads and 100μm for RF pads. Total area consumption of this chip is $1.8 * 1.8mm^2$ which includes LNA and active gilbert cell down conversion mixer

circuits and pad ring. Complete LNA and integrated mixer layout (GDSII generated) is shwon in Fig. 4.12.

4.4.1 Measurement Results of Auxiliary Receiver

Measurement setup

Fabricated die microphotograph is shown in Fig. 4.13. Measurements were done on a PCB with packaged dies as well encapsulated chip-on-board (module) as shown in Fig 4.14(a) and Fig 4.14(b). The board has differential RF inputs and differential fLO inputs. Off-board (Marki microwave) baluns were used to provide differential drives. At the output of the receiver differential buffer was added to isolate the loading effects seen in the mixer output stage, a off chip IF balun (mini circuit) is used for differential-to-single-ended measurement. The test boards was built with FR4 material. Fig. 4.14(a) and Fig. 4.14(b) shows a complete photograph of the assembled test board and module (chip on board). Agilent DC power supplies are used for DC characterisation. Agilent Vector Network Analyser (VNA), E8538 is used for LO signal generation and Rohde and Schwarz AMU200A base band signal generator is used for RF signal generation. Agilent noise figure analyser, N8975A is used for noise figure measurement.

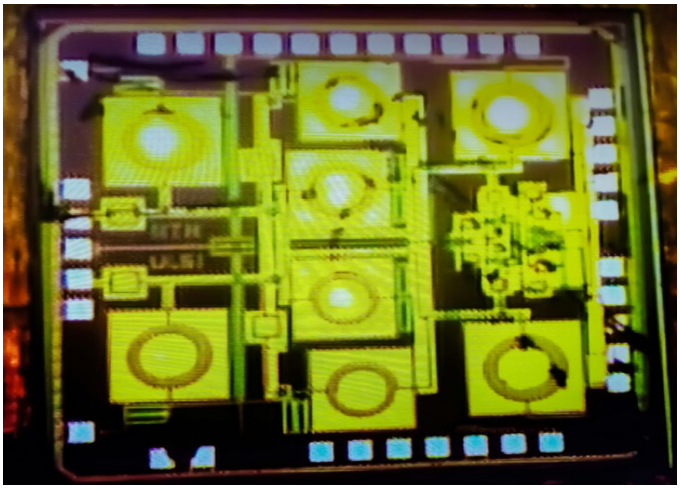
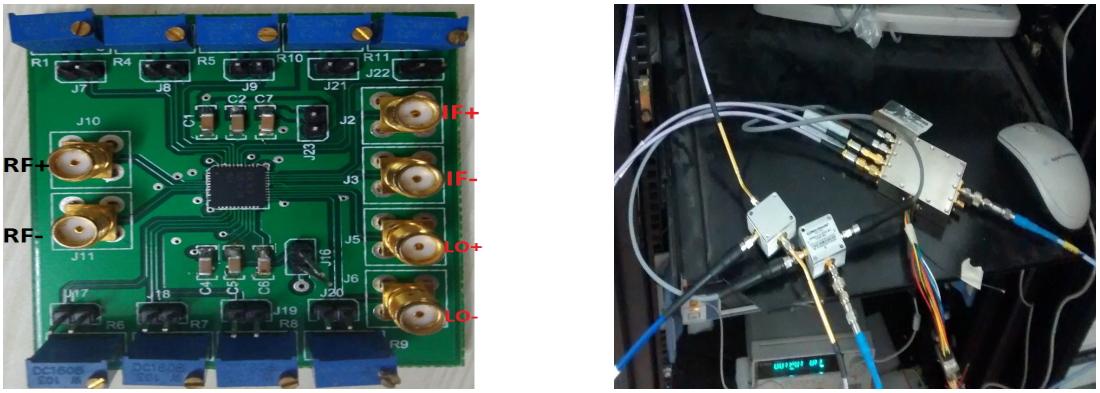


Figure 4.13: Die photograph of Subthreshold receiver



(a) Assembled test board.

(b) module (chip on board).

Figure 4.14: Assembled test board and module

Result and Discussion

The chip consumes 7.5 mA at 2 GHz fLO and 7.8 mA at 5 GHz fLO from a 1.8 V voltage supply including all the currents drawn from bias circuitry. The fLO signal needs to be 0 dBm at 2 GHz and 2 dBm at 5 GHz in order to maintain front-end functionality. These power levels are measured at the SMA connector inputs.

Fig. 4.15 shows plots of the input reflection (S_{11}) referring to a 50Ω differential source impedance. The S_{11} measurements were done throughout the frequency range. S_{11} matches better than -10 dB from 2.2 GHz to 5 GHz. In the 2G to 5G, S_{11} matches better than -8 dB. The S_{11} results include parasitics due to the connector and test boards. The results suggest that the designed front-end requires two RF balun and one IF balun for the intended application.

Fig. 4.16(a) shows conversion gain at a function of LO frequency for baseband frequencies of 50 MHz. The LO frequency in this measurement is sweeped with RF at difference of 50MHz. The results include variations due to impedance mismatches at the LNA inputs. The voltage gain of the front-end is approximately 3 dB lower than the power gain. IF spectrum taken from spectrum analyzer is shown in Fig. 4.16(b) at 2G RF frequency with single ended output @−32dbm input power, So differential is +6dB and cable and balun loss is around 4.9dB. Thus by looking conversion gain plot it is perfectly matching with simulation results.

Noise was measured at various LO and RF frequencies using a noise figure meter. At 2

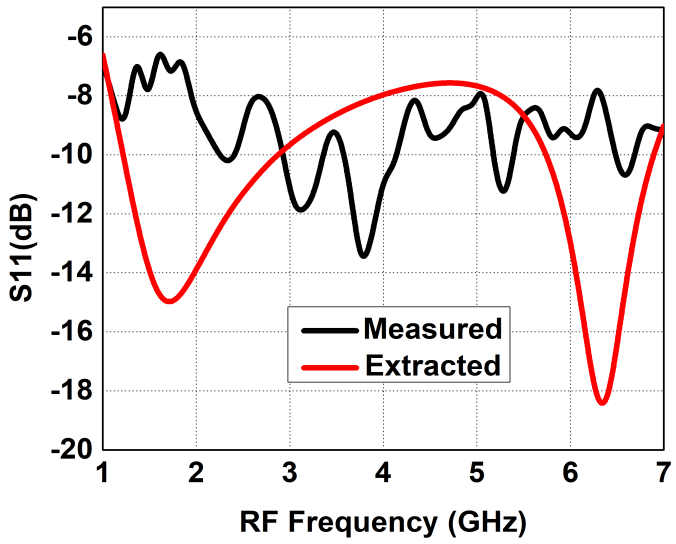
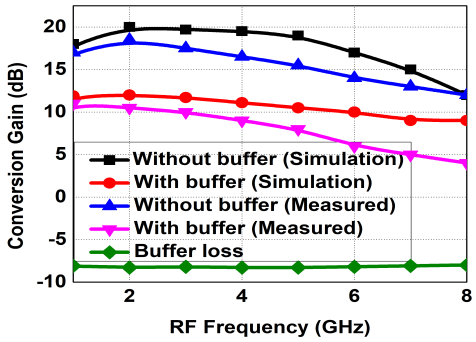
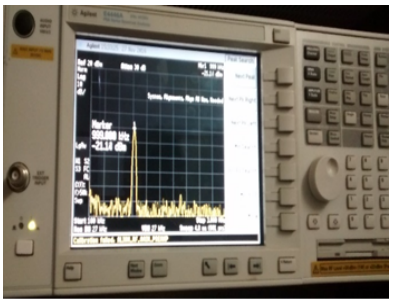


Figure 4.15: S11 of Subthreshold (Auxiliary) Receiver



(a) Conversion gain of receiver at 50MHz IF frequency.



(b) Single ended IF spectrum at spectrum analyzer @−23dBm input power.

Figure 4.16: Measured Conversion gain of subthreshold receiver @ 50MHz IF frequency

GHz fLO and 50 MHz baseband, the measured double-sideband noise figure (DSB NF) is 12 dB encluding all the balun, cable, board losses, and input mismatches. The estimated loss of the balun and cable (obtained from separate cable and balun measurements using a network analyzer) is 3.1 dB, and the de-embedded DSB NF is 12 dB − 3.1 dB = 8.9 dB. The 8.9 dB DSB NF still includes any board and SMA connector losses, since it is not possible to directly measure the loss on the PCB. Plots of de-embedded NF versus baseband for various RF bands are shown in Fig. 4.17. DSB NF is approximately 9 dB at 2 GHz RF and 50 MHz baseband.

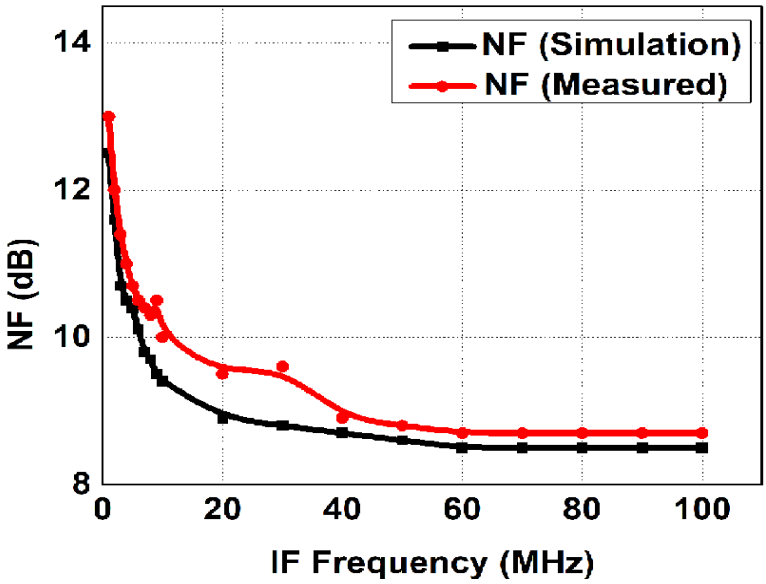


Figure 4.17: Measured noise figure of subthreshold receiver

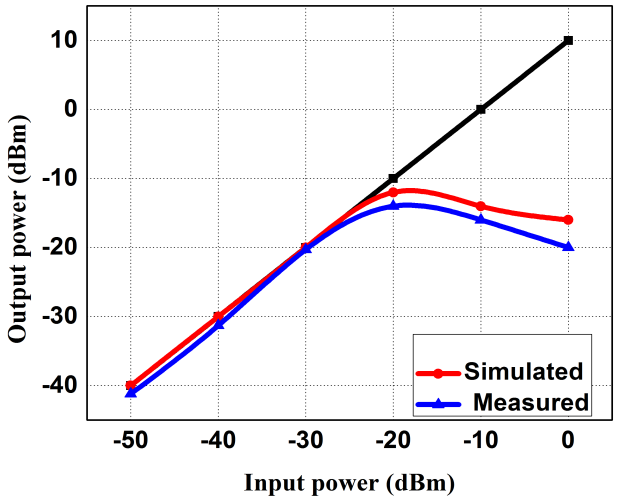


Figure 4.18: Measured 1dB-CP of subthreshold receiver

The 1 dB compression point (P-1dB) of the circuit is limited by the output swing and varies with the frequency offset of the blocking signals. 2GHz fLO, the measured input-referred P-1dB at 1MHz is -21 dBm. Fig. 4.18 shows the measured and simulated 1 dB compression point. At the input power of -26 dBm, the output voltage is approximately 0.7 Vp-p on each side of the

differential outputs. At this condition, the gain of the receiver drops rapidly as a function of Vout amplitude, and the compression is caused by higher-order distortions .

4.5 Performance Summary

Performance summary is shown in Table 4.4.

Table 4.4: Performance summary with comparison of subthreshold receiver

Ref.	Freq. (GHz)	A_v (dB)	S_{11}	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)	FoM
[69]MWCL 2008	3-5	22.2	<-10	17	-6	2	16	180	11.9
[55]ISOCC 2012	2545-2700	8.89	<-19	8.85	-9.5	1.2	3.12	180	4.3
[56]JSSC 2014	0.433/0.860 0.915/0.960	50±2	<-10	8.1±0.6	1.15±0.05	0.5	1.15±0.05	65	14
[57]MWCL 2015	0.85-2.55	55	<-8	13.6	-7.5	0.8	0.53-0.97	28	7980
[70]VLSI 2017	1-5	35	-7.5	2.7	-6	0.4	10	16	35.5
This Work. (Post layout Simulation)	2-5	19.5-18 @-47	<-10	8.5	-21(1dB)	1.8	3.02	180	370.2
This Work* (Packaged Measurement)	2-5	8.9-9.12 @-23	<-10		-22(1dB)	1.8	3.5	180	260.46
This Work* (Chip on Board)	2-5	19-16 @-23	<-10	8.6-9	-20(1dB)	1.8	3.2	180	300
*Sensitivity = -90dBm									
*Sumulation RF input power = -47dBm *Measurement RF input power = -23dBm									

$$FoM = \frac{A_v(lin) * BW(GHz) * Gatelength(nm)}{Current(mA) * NF(lin)} \tag{4.15}$$

A Figure of Merit (FoM) given in (4.15) suitable for evaluating for the proposed high performance receiver is given in Table 4.4 and the same is calculated for the related recent works as given in Table 4.4. Though [57] has more FoM, it is a mixer first receiver and becomes a frequency selective wideband architecture. However, the proposed architecture has continuous wideband with better noise figure and state of the art, best reported subthreshold receiver covering 2GHz -5GHz frequency band. Buffer loss has been de-embeded for all tabulated results listed in Table 4.4.

4.6 Summary

This chapter has explored various techniques for implementing very low power ultra wideband receiverin CMOS subthreshold region operation. In this context, a gilbert cell mixer with RC degeneration had introduced to enhance RF bandwidth. Effect of gilbert cell mixer with RC degeneration on various performance parameter has been analyzed in detail. Complete mathematical analysis of this technique is presented and the same is verified by designing an WB down conversion mixer. Finally, a ultra low power wide band receiver is designed, simulated and measured in 180nm CMOS technology for out of band sensing. Its performance is compared with other receiver tabulated above. Thus the proposed architecture is the most suitable one for realization and overall figure of merit.

Chapter 5

Reconfigurable Mixers for RF Front End

5.1 Introduction

A number of broadband receivers and transceivers have been demonstrated in recent years [71] [72] [73] [74] [75]. However, the design of broadband reconfigurable receiver for transceivers is still a work in progress. Many open problems remain, and are worthy of intensive research. Emerging Internet of Things (IoT) enabled platform demands multi-mode multi-standard transceivers to enhance the performance through seamless connectivity between zigbee, bluetooth, Wi-Fi, UWB and cognitive radio interface. The easiest solution is to put multiple separate radio to above need [41] [76], however, in real scenario only one of the mode function at a time. So above approach is power hungry, costly and take more area. Therefore, to get a cost effective solution, a re-configurable single radio (that can configure to multi-mode as need basis) would be the best choice. To make the radio reconfigurable researchers introduce the RF transceiver front-end with reconfigurable LNA [77], PA, PLL [78], mixer [79] [80] [81], and filter [43] etc. Among them, our emphasis is to design a Mixer that can provide reconfigurlibity on the performances like gain, linearity , noise figure and bandwidth selection. Most of proposed reconfigurable mixer have

shown gain variability and Bandwidth tuning [82]- [83] through current variation, load tuning etc [84]- [80]. In such designs, multi channel sensing and signal strength adaptability are the main target and are designed for single standard operation. However, in multi-mode IoT systems, the other performances like noise figure, linearity reconfiguration are need to be incorporated in mixer design. In this regard, we propose a re-configurable down conversion mixers with different reconfigurability.

Table 5.1: Review of recent reconfigurable wideband LNA and mixer

Ref.	Circuit	Freq. (GHz)	A_v (dB)	NF (dB)	IIP_3 (dBm)	VDD (Volts)	P_{DC} (mW)	Tech. (nm)
[79]	Reconfigurable AM	0.7-2.3	4-22	8	8.5	1.8	5.58-10.08	180
[80]	Reconfigurable PM	1-12	1.2-17	11	8.6	1.2	5.9	
[77]	Reconfigurable LNA	0.5-2	14.7-23	2.7-4	-10 -9.4	1.2	12.4-17	90
		2-6	12-22.5	2.8-3.9	-11-10.4	1.2	10.8-18.2	90
[81]	Passive	0.15-0.85	51±1	4.6 ± 0.9	17.4	1.2,2.5	10.6-16.2	65
	Active	0.15-0.85	51±1	4.6±0.9	-12	1.2,2.5	10.6-16.2	65

5.2 Wide-Band Reconfigurable (Active / Passive) Down Conversion Mixer

A 1.2V proposed reconfigurable down conversion mixer which is switchable between active and passive mode shown in Fig. 5.1 is designed in UMC 65nm CMOS Technology.

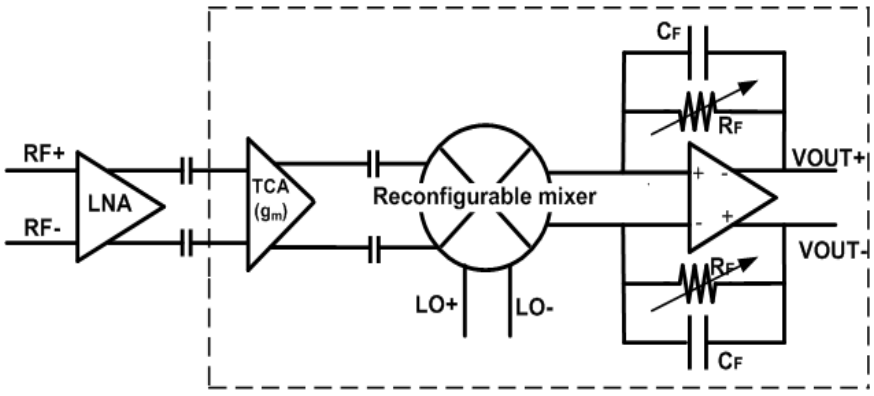


Figure 5.1: Wide-band reconfigurable down conversion mixer

Reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The

CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. Hence this circuit will be much helpful in multi-standard receiver design in IoT perspective.

5.2.1 Transconductance Amplifier

Fig. 5.2 shows the transconductance stage of the mixer. It consists of a differential complementary pair and a common-mode feedback circuit. The RF and the LO signals are AC-coupled into the mixer core through linear metal-insulator metal (MIM) capacitors. AC coupling increases biasing flexibility and suppresses low frequency distortion interaction between stages. The current from the transconductance stage, however, is DC-coupled to the switching pairs. We realize minimum parasitic capacitance at the transconductance stage output, C_{par}, if there is no capacitor between the stages (used for DC blocking) by reducing the signal routing.

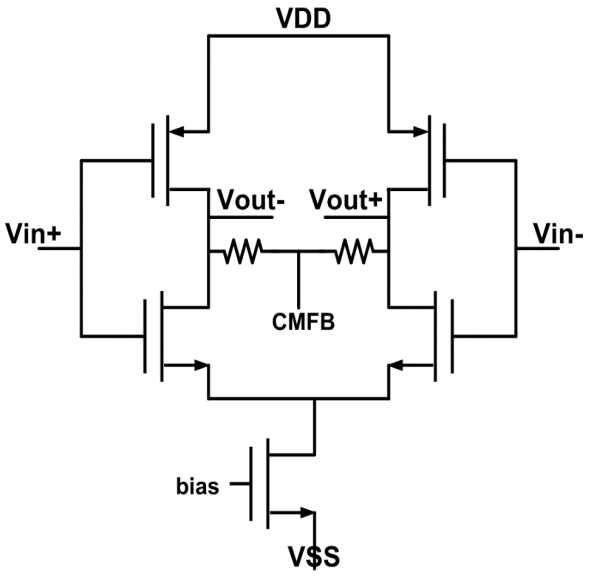


Figure 5.2: Transconductance Amplifier

On the other hand, the absence of DC blocking capacitors results in non-zero DC bias current flowing through the switches. This current should be minimized in order to reduce 1/f noise contributions from the switches, and this was done by careful design of common-mode feedback circuits in both the opamp and the transconductor. Since there is no AC coupling capacitor

between switching stage and OPAMP, low frequency intermodulation tones created by second-order nonlinearity (due to mismatches) will transfer to the next stages downstream. Thus it is important to reduce the second-order nonlinearity in this stage by using a fully differential topology. Although using the fully differential topology requires extra headroom for the pair due to current-source biasing, the RF voltage swings at this stage are low due to the virtual ground set by an operational amplifier. The NMOS and PMOS devices are biased at the high overdrive Vgs-Vth region in order to achieve high linearity. The common-mode voltages at the mixer and the operational amplifier outputs are set at Vdd/2 in order to obtain the highest possible headroom for voltage swing.

5.2.2 Common Source Reconfigurable Mixer

Modulator circuit is reconfigured between active and passive modes by switching between the output load, DC power supply and Gm stage (Gm MOS of active case) and current source shown in Fig. 5.3. Common source configuration is chosen because of compatibility with cases. In passive mode, the frequency mixer or modulator circuit is simply composed of four NMOS transistors characterized by resistance (Ron) when switched on. Accordingly, in order to make the common-source input stage configuration suitable for both active and passive mode topologies, switch (Sw1-2) are implemented using PMOS which have been added between the gate and drain of the common source transistor (Gm MOS)as shown in Fig. 5.3. TCA differential output current is applied at the drain of the transistor Mp1 and Mp2 (PMOS switch 1-2) to route to the mixer core for mixing in the current domain. Vlogic high or low is given to Mp1 and Mp2 to configure reconfigurable mixer to operate in an active/passive mode as shown in Fig. 5.4. Specifically when there is no current flowing through the mixer core, Vlogic is set to zero, thus causing input signal to flow directly through the switching stage as shown in path 1 to mix with LO signal. Width of PMOS is chosen to provide degeneration resistance, thus turning the overall mixer topology into a passive mode as shown in Fig. 5.6(a). Transistors thus operate as switch 1-2 as well as degeneration resistance R_{deg}(switch 1-2 resistance), thereby increasing linearity of passive mixer [85]. Capacitor Cc is a high-frequency compensation capacitor used to suppress the noise at higher frequency. The output signal is supplied from the mixer core without any

load and directly coupled with transimpedance amplifier. The voltage conversion gain of passive mixer is

$$VCG = \frac{2}{\Pi} * g_m * Z_f \tag{5.1}$$

where Z_f is the feedback impedance of transimpedance amplifier, $C_F \mid\mid R_F$ and gm is the transconductance of transconductance amplifier.

Resistive switches 3-4 designed using transmission gate, made of PMOS and NMOS switch, are fully turned off ensuring that output current of switching quad directly goes to the transimpedance amplifier without any coupling capacitor. Switches 5-7 designed using NMOS will also be off when this circuit operates in passive mode.

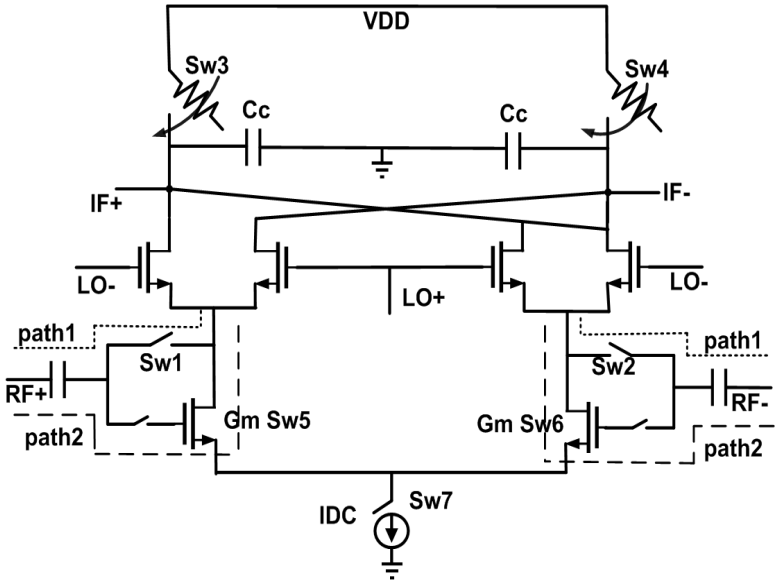


Figure 5.3: Reconfigurable down conversion mixer

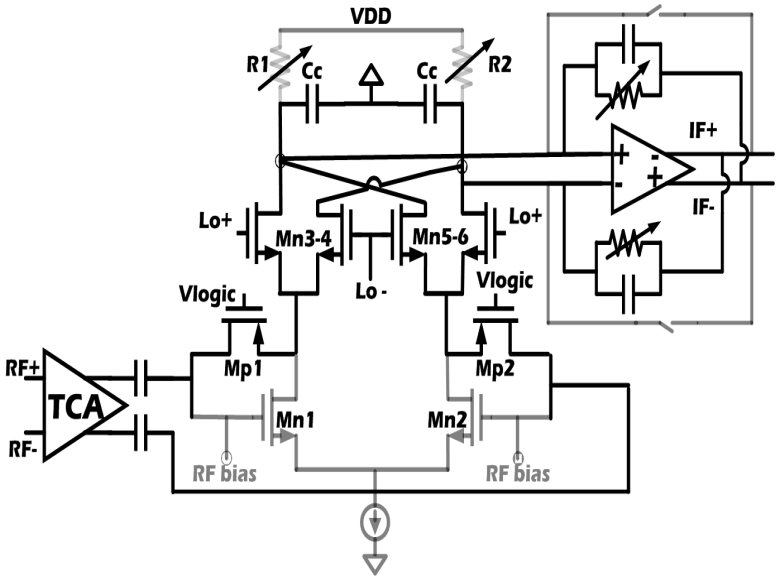


Figure 5.4: Passive mode

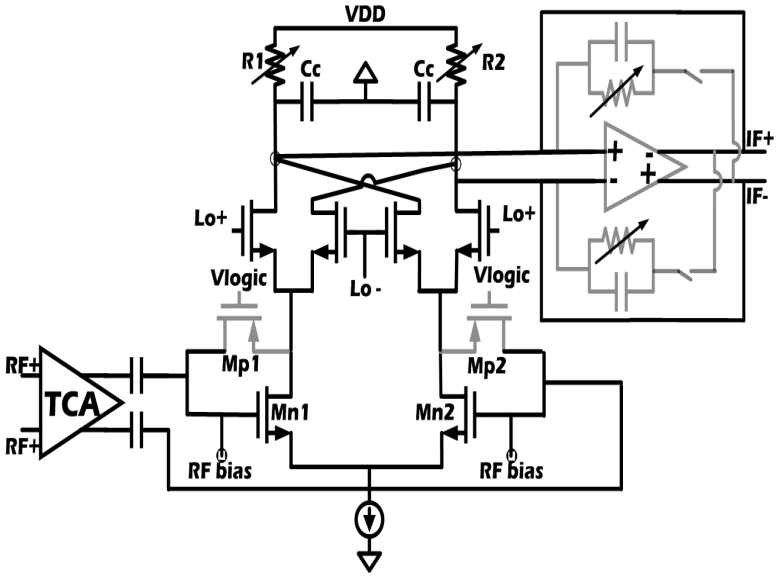


Figure 5.5: Active mode

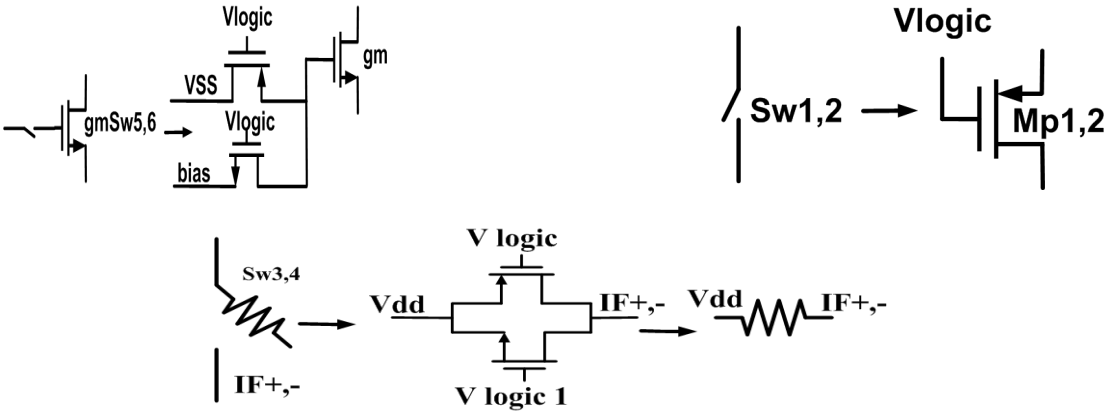


Figure 5.6: Switch Implementation

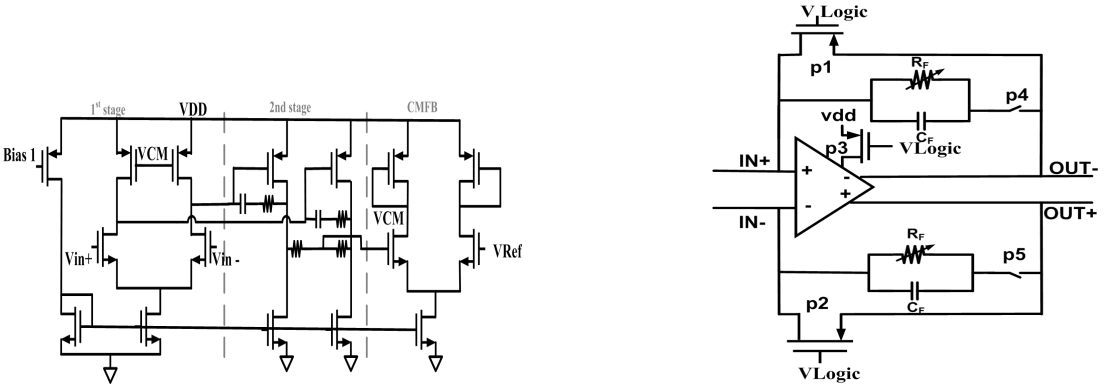
In active mode, input stage of the frequency mixer or modulator circuit have a configuration that is a common source topology. This topology is chosen to provide better gain and low noise figure. Double balance gilbert cell architecture is used in active configuration when there is current flowing through input(Gm) MOS Mn1 and Mn2 (Sw 5-6). The bias voltage can be selected to control parameters of input stage or switching operation of Gm MOS switch 5-6 as shown in path 2. The Gm of MOS Mn1 and Mn2 can be changed by changing the value of bias voltage, thus varying the gain of mixer. The optimum value of bias voltage is desired to consumes a minimal amount of current. Switch 7 has been designed using NMOS which is biased in saturation region to provide current source. Thus turning the overall topology into an active mode as shown in Fig. 5.5

Transmission gate is used as a resistive switch connected between VDD and IF output as shown in Fig. 5.6(c). W/L of PMOS and NMOS is chosen so that some voltage drop occurs across it and act as a resistance. Transmission gate total resistance is Rtol = RPMOS||RNMOS. As it is connected to VDD so it acts as resistive load and Capacitor Cc is provided to act as a low pass filter in active mode operation of reconfigurable mixer. Gain of active mixer can be tuned by changing the resistance of transmission gate. The output of active mixer is directly passed to the output stage without going to TIA.

5.2.3 Transimpedance Amplifier

A simplified schematic of transimpedance amplifier is shown in Fig. 5.7(b). TIA consists of an operational transconductance amplifier with a feedback $R_F C_F$. R_F and C_F value is set according to IF frequency. A two stage miller compensated OTA topology is chosen for TIA design as shown in Fig. 5.7(a). First stage to provide high gain and second stage for high swing. So that structure can obtain both, high output swing and low input referred noise. Transimpedance amplifier is used to convert current to voltage output in passive mode operation. The TIA stage serves as load and anti-aliasing filter for the passive mixer. The TIA is designed in such a way so that very low impedance is provided at the passive mixer output. TIA input impedance is given by

$$Z_{in}(f) = \frac{2}{A(f)} * \frac{R_F}{1 + 2\Pi * R_F C_F} \tag{5.2}$$



(a) Two stage miller compensated OPAMP

(b) Transimpedance Amplifier

Figure 5.7: Transimpedamce Amplifier

Where A(f) is the open loop gain of the OTA. Due to high gain OTA bandwidth is limited and high frequency components suffer high impedance. In order to filter out high frequency components CF is inserted. This is done for all signal current to flow into feedback $R_F C_F$ from the mixer core. The TIA draws a total of 3.3mA from the supply. In case of active mixer operation TIA will be switched off to save power. In case of active mixer operation TIA will be switched off by switching off p3 switch to save power and p1, p2 will be on. p4 and p5 also implemented using MOS and switch on or off in case of passive and active respectively. The gain

of the TIA can be tuned by changing the value of R_F and it provides another degree of freedom to configure the gain of the downconverter.

5.2.4 Simulated results

Based on the qualitative description of the building blocks, using their insights related to operation, the RF front-end demodulator is simulated and extracted shown in Fig. 5.24 in CMOS 65nm process. The voltage conversion gain plot is shown in Fig. 5.21 with respect to RF frequency at 5MHz IF. The voltage conversion gain is close to 29.2dB and 25.5dB for active and passive case respectively. The simulated double side band noise figure at 2.45GHz is shown in Fig. 5.9. In addition, the corner frequency is less than 100KHz and 200KHz in passive mode and active case operation respectively. Simulated noise figure for active and passive is 7.6dB and 10.2dB @ 5MHz respectively.

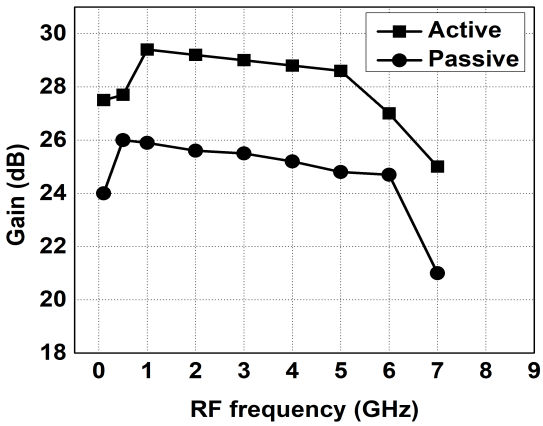


Figure 5.8: Simulated conversion gain reconfigurable mixer vs RF frequency.

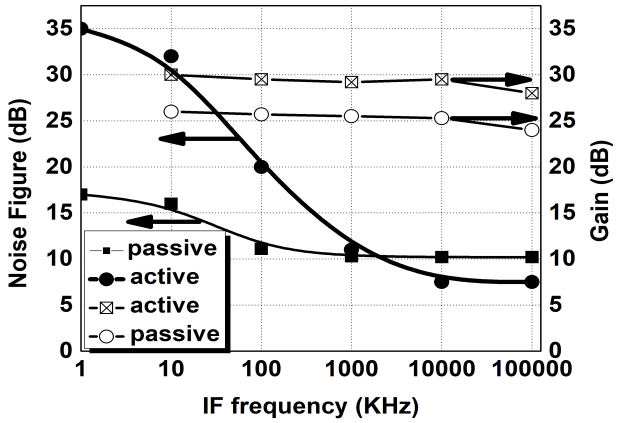
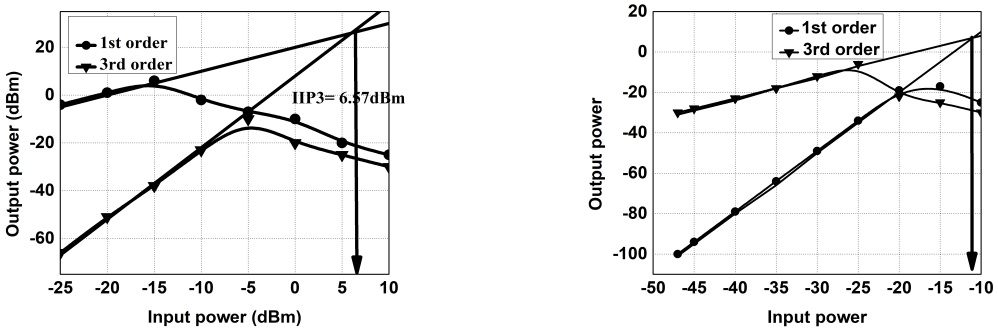


Figure 5.9: Simulated noise figure and conversion gain vs IF frequency.



(a) IIP_3 of passive mixer.

(b) IIP_3 of active mixer.

Figure 5.10: Simulated linearity of reconfigurable mixer

The two tone linearity test result is shown in Fig. 5.10(a) for 2.4GHz LO frequency. Due to high conversion gain at low IF, the output compression point of the OPAMP, limits the input referred linearity of the circuit. 1dB-compression point of the circuit is limited by the output swing and varies with IF frequency. The simulated IIP3 in case of passive is 6.57dBm and 1dB compression of active at RF frequency 2.45GHz is shown in Fig. 5.10(b). 1dB-CP of active is -24.5dBm.

A Figure of Merit (FoM) given in chapter 4 suitable for evaluating the proposed reconfigurable down conversion mixer is given in Table 5.2 and the same is calculated for the related recent

Table 5.2: Simulation results of Reconfigurable mixer and Comparison

Parameters	Active** (This work)	Passive*** (This work)	[76]AM	[44]PM	[41]PM	[84]RAM	[79]RPM
Gain (dB)	29.2	25.5	14.5	13	22.5-25	1.2-17	3.5-20.5
NF (dB)	7.7	10.2	6.5	13.7	7.7-9.5	≥ 11	≥ 8
IIP_3 (dBm)	-11.9	6.57	NA	≥ 10.8	≥ 7	8.6	≤ 8.5
Power(mW)	9.36	9.24	14.4	8.04	10*	5.9	5.6-9.6
BW(GHz)	1-5.5	0.5-5.1	1-10.5	900M 1.8-2.5	1.55-2.3	1-12	.7-2.3
CMOS Tech.	65nm	65nm	65nm	65nm	180nm	130nm	180nm
Supply	1.2V	1.2V	1.2	1.2	2	1.2	1.8
FoM	172.12	64.46	56	1.19	37.71	73.77	41.3
*(mixer+TIA)							
LO to RF isolation (-60** , -90***)							
LO to IF isolation (-70**, -100.5***)							

works as given in Table 5.2. Reconfigurable down conversion mixer in active mode has the better FOM as compare to other. Therefore it is clear that the architecture as proposed above is best suited for the realization of multiband IoT application

5.3 A Low/High Band Parallel path TCA with configurable (Active / Passive) Down Conversion Mixer

Down conversion mixer described in section 5.2 has configurability between active and passive modes with gain and noise tunability but there is no configurability in RF bandwidth. To Reconfigure RF bandwidth, a down conversion mixer for a multistandard wireless receiver, with adapted reconfigurability in the form of RF bandwidth, active/passive and IF bandwidth is shown in Fig. 5.11. In the proposed architecture RF bandwidth reconfigurability is reconfigured between low band (LB) RF frequency and high band (HB) RF frequency mixer modes. LB / HB reconfigurability is made through power switching the transconductance amplifier. Active / Passive reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. The proposed circuit is designed in the UMC 65nm RFCMOS technology with 1.2V supply voltage.

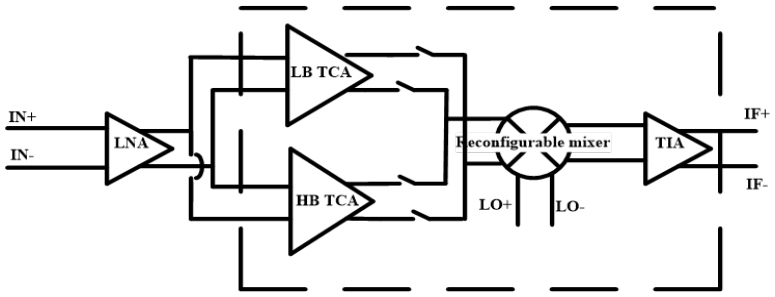
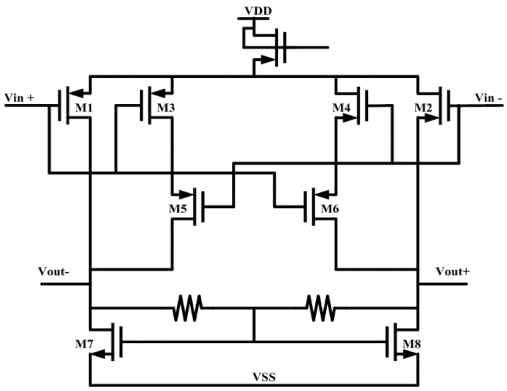


Figure 5.11: Low/High Band Parallel path TCA with configurable (Active / Passive) Down Conversion Mixer.

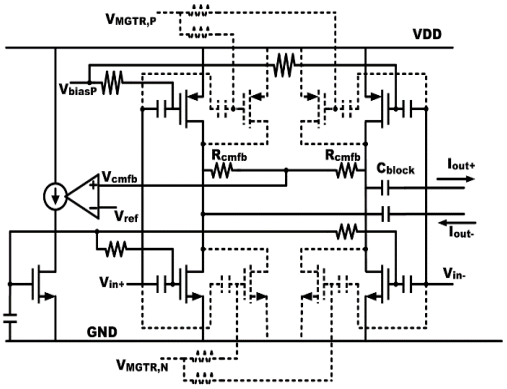
5.3.1 Transconductance Amplifier

A current switching passive mixer consists of transconductance stage, switching stage and transimpedance amplifier stage. Fully differential CMOS transconductors are employed for LB and HB to convert the input RF voltage signal to RF current as shown in Fig. 5.12. Post which the current signal is fed to the switching stage ensuring that second order nonlinearity is reduced by using fully differential topology. TCA is modeled to minimize the signal loss and enhance its linearity performance. Fig. 5.12(a) shows a simplified circuit schematic of the gm stage, where the main transistor pair M1 and M2 and auxiliary circuit M3-M6 are designed using PMOS that cancel the third order distortion of the main pair [86]. The gm stage is designed to dissipate 2.7mA current from a 1.2V supply with .1 to 1.5G bandwidth. Both PMOS and NMOS input stages use balanced input devices with no tail current as shown in Fig. 5.12(b). The use of multi-gated [41] input pair allows tuning to be done to achieve higher IIP3 with almost same bias current. HB gm stage is designed to work from .6 to 5GHz. and dissipate 5.2mA current.

The common mode voltage is designed at VDD/2 for getting maximum swing. By setting VDD/2 common mode voltage, current can be minimized and parasitic capacitance at the output nodes of transconductor is optimized to the smallest possible value, thereby increasing the output impedance, for the purpose of improving the noise figure. The transconductance stage gain also reduces the overall noise of front end receiver.



(a) Low band Transconductance Amplifier.



(b) High band Transconductance Amplifier.

Figure 5.12: Low / High band Transconductance Amplifier

5.3.2 Active/Passive Mixer

In this embodiment, modulator circuit is reconfigured between active and passive modes by switching between the output load, DC power supply and Gm stage (Gm MOS of active case) and current source as shown in Fig. 5.3. Common source configuration is chosen because of compatibility with cases. Functionality is same explained above. Functionality of active / passive mixer will remain same as explained in section 5.2.2.

5.3.3 Transimpedance Amplifier

It consist of two stage miller compensated OPAMP which is similar to the topology shown in Fig. 5.7. Same mechanism is used as discussed above in section 5.2.3 for active/ passive.

5.3.4 Simulated Result

The downconversion mixer is designed in UMC 65nm Technology with 1.2 V supply. Based on the qualitative description of the building blocks, using their insights related to operation, all simulation results are compared. Fig. 5.13 shows conversion gain (in high-gain mode and low gain mode) at a function of LO frequency for baseband frequencies of 1 MHz. The voltage conversion gain is close to 22/26 dB and 25/31 for LB and HB case respectively where these figures suggest passive/active (PLB, PHB, ALB, AHB) mode. The simulated double side band noise figure at

800MHz and 2GHz for LB and HB respectively is shown in Fig. 5.14. The Simulated noise figure for active/passive is 14.2/12.1 dB and 11.5/8.16 dB @ 5MHz in LB and HB case respectively.

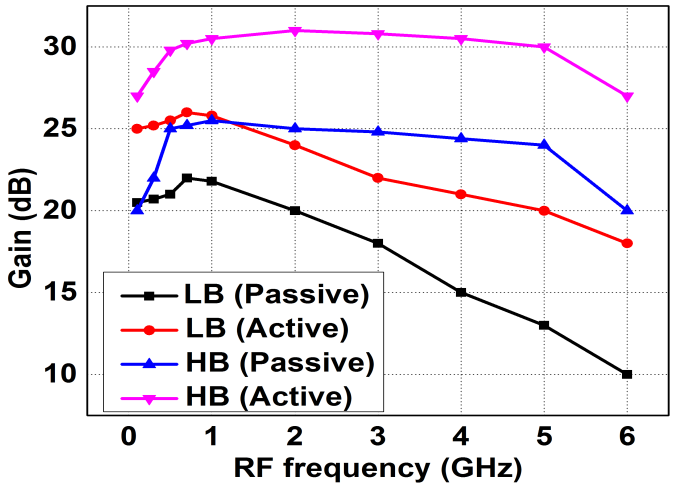


Figure 5.13: Simulated conversion gain reconfigurable mixer vs RF frequency.

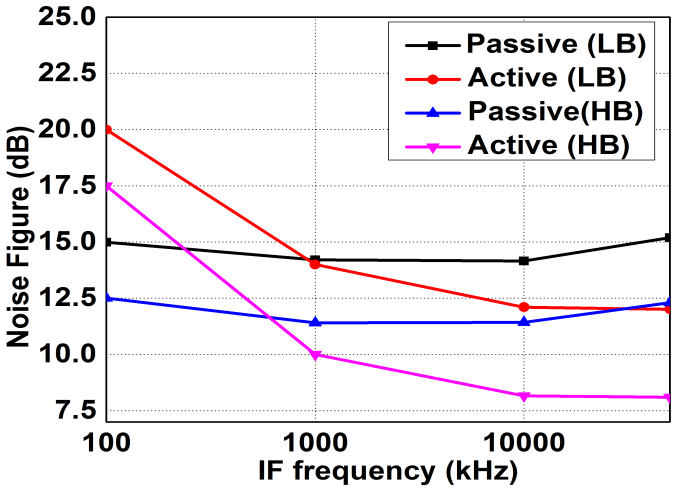
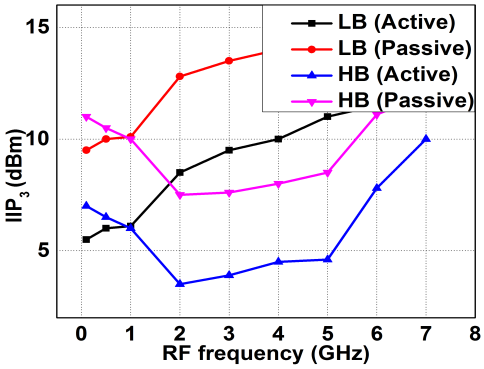
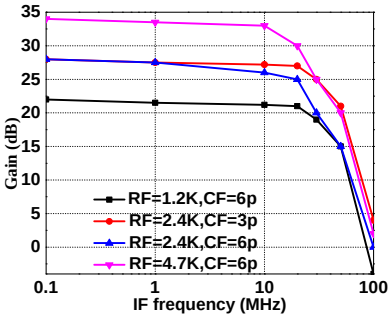


Figure 5.14: Simulated noise figure vs IF frequency.

The two tone linearity test result is shown in Fig. 5.15(a) for 2GHz and 800MHz LO frequency for HB and LB. Due to high conversion gain at low IF, the output compression point of the OPAMP, limits the input referred linearity of the circuit. 1dB-compression point of the circuit is limited by the output swing and varies with IF frequency. The simulated IIP3 is 6.4/3dBm and 10/8.1 for HB and LB, where these figures suggest passive/active mode



(a) IIP_3 of Reconfigurable mixer.



(b) Voltage Conversion Gain of Reconfigurable mixer.

Figure 5.15: Simulated linearity and Gain of reconfigurable mixer

Fig. 5.15(b) depicts the voltage conversion gain of the proposed down conversion passive mixer of LB. By changing the value of R_F and C_F gain can be varied with constant bandwidth or by varying only R_F, conversion gain can be varied with little variation in bandwidth.

Table 5.3: Simulation results of Low/High Band Parallel path TCA with configurable (Active / Passive) Down Conversion Mixer and Comparison

Parameters	ALB* T.W.	AHB* T.W.	PLB* T.W.	PHB* TW	[42]PM	[86]PM	[87]RAM	[79]RPM
Gain (dB)	26	31	22	26	19.5-21	22.5-25	1.2-17	3.5-20.5
NF (dB)	12.1	8.16	14.2	11.4	11.4-12.4	7.7-9.5	≥ 11	≥ 8
IIP_3 (dBm)	8.1	3	10	6.4	8-9	≥ 7	8.6	≤ 8.5
Power(mW)	7.17	10.66	7.05	10.56	5.4	10	5.9	5.6-9.6
BW(GHz)	.1-1.5	.6-5	.1-1.5	.6-5	.048-.86	1.55-2.3	1-12	.7-2.3
Tech.	65nm	65nm	65nm	65nm	180nm	130nm	130nm	180nm
Supply	1.2V	1.2V	1.2	1.2	1.2	2	1.2	1.8
FoM	5.975	163.7	6.92	43.3	13.5	37.71	73.77	41.3
ALB* - Active Low Band, AHB* - Active High Band PLB* - Passive Low Band. PHB* - Passive High Band								

A Figure of Merit (FoM) given in chapter 4 suitable for evaluating the proposed reconfigurable down conversion mixer is given in Table 5.3 and the same is calculated for the related recent works as given in Table 5.3. Reconfigurable down conversion mixer in active mode has the better FOM as compare to other and other cases are also it is comparable. Thus the proposed architecture is the better fit for realization and overall figure of merit.

5.4 Reconfigurable High/Low band Passive Down Conversion mixer for wide band Receiver

In section 5.3 RF configurability is done by power switching HB/LB transconductance amplifier. Further to reduce the area of the chip down conversion mixer RF bandwidth reconfigurability is reconfigured between low band (LB) RF frequency and high band (HB) RF frequency mixer modes is shown in Fig. 5.16. LB / HB reconfigurability is made through PMOS/NMOS switching the transconductance amplifier between these two modes. The proposed circuit is designed in UMC 65nm RFCMOS technology with 1.2V supply voltage. This circuit provides bandwidth configurability in single circuitry without increasing power consumption.

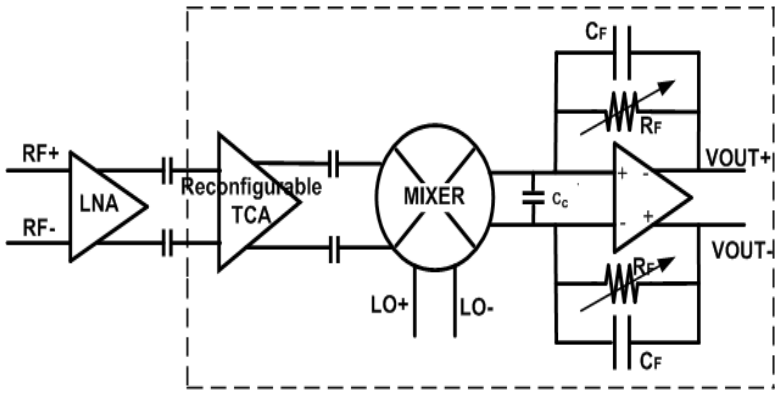


Figure 5.16: Reconfigurable High/Low band Passive Down Conversion mixer .

5.4.1 Transconductance Amplifier

A current switching passive mixer consists of transconductance stage, switching stage and transimpedance amplifier stage. Fully differential CMOS transconductance stage is employed for LB and HB to convert the input RF voltage signal to RF current as shown in Fig. 5.17. Post which the current signal is fed to the switching stage ensuring that second order nonlinearity is reduced by using fully differential topology. TCA is modeled to minimize the signal loss and enhance its linearity performance.

Fig. 5.18(a) shows a simplified circuit schematic of the low band (100M - 500M) transconductance stage of mixer, when all four switches(s1-s4) are on and M_{n8} is off to get symmetry to

cancel common mode noise. It consists of a differential pair and a common-mode feedback circuit to keep the output voltage as half of VDD. It is necessary to increase the transconductance of the G_m stage because the loss at the following passive switching stage degrades the overall mixer NF. In order to achieve high gain with low power consumption, gm stage adopts current reused complementary input which boosts up transconductance by 2 times. Another advantage of complementary input is that input nMOS and PMOS can have same DC bias level so that input capacitors for DC bias level separation between nMOS and pMOS are not required. [88]. It also consists of an auxiliary transistor (M_{p3} -M_{p6}), main transistor (M_{p1} - M_{p2}) and for complementary input auxiliary and main transistor ($Mn3$ - $Mn6$) (M_{n1} - M_{n2}) respectively, which cancels the third order linearity. The gm stage is designed to dissipate 690uA current from a 1.2V supply with 100M to 500M RF bandwidth.

High band transconductange stage of down-conversion mixer is shown in Fig. 5.18(b) [41], where all four switches(s1-s4) are off and M_{n8} is on. It consists of a differential complementary pair with common mode feedback VDD/2. It is important to reduce the second order nonlinearity in this stage by using fully differential topology. HB gm stage is designed to work from 0.6 to 5GHz ans it dissipated 5.9mA current.

Two separate common mode feedback is used for LB / HB. By setting VDD/2 common mode voltage, current can be minimized and parasitic capacitance at the output nodes of transconductor is optimized to the smallest possible value thereby increasing the output impedance, for the purpose of improving the noise figure. Transconductance stage gain also reduces the overall noise of front end receiver. All switches are controlled by single logic that is controlled by simple inverter. Either logic 0 or logic 1 is applied according to the on/off requirement.

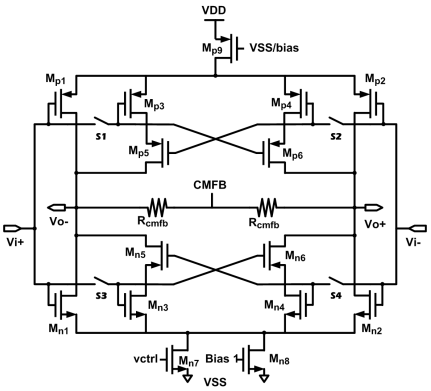
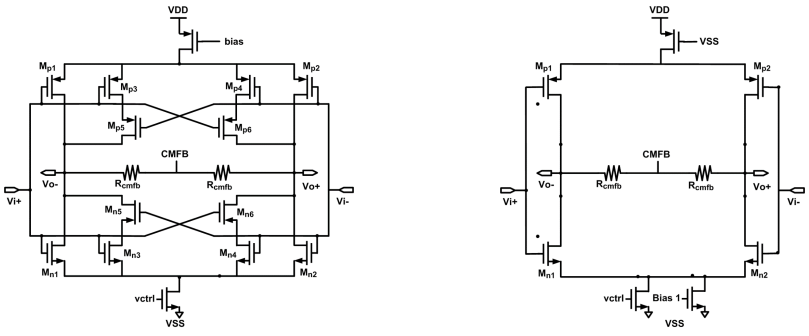


Figure 5.17: Reconfigurable High/Low band Transconductance Amplifier .



(a) Low Band Transconductance Amplifier.

(b) High Band Transconductance Amplifier.

Figure 5.18: Low / High Band reconfigurable Transconductance Amplifier

5.4.2 Switches

Switches consists of four transistors forming a double balanced structure with two degeneration MOS transistors as shown in Fig. 5.19. LO signals are AC coupled via capacitors while DC bias level of the switches is set such as to achieve the lowest on resistance while preventing overlapping on periods. The switches should be sized big enough in order to minimize the on-resistance. However, LO power consumption as well as noise contributions from the operational amplifier determine an upper limit on the size due to parasitic capacitances. R_{deg} is the degeneration resistance Cc is the high frequency compensation capacitance. By degeneration resistance equivalent resistance of mixer can be increased and current splitting can be more balanced [42] and

Conversion gain of mixer is defined as given in (5.1).

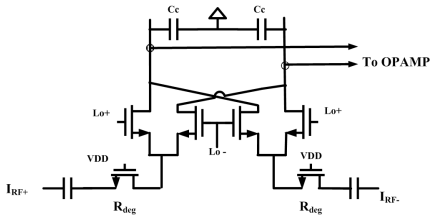


Figure 5.19: Switching Quad with degeneration resistance

5.4.3 Transimpedance Amplifier

Transimpedance amplifier consists of an operational transconductance amplifier with a feedback R_F, C_F. R_F and C_F value is set according to IF frequency. A two stage miller compensated OTA topology is chosen for TIA design as shown in Fig. 5.20. First stage to provide high gain and second stage for high swing. So that structure can obtain both, high output swing and low input referred noise. Transimpedance amplifier is used to convert current to voltage output in passive mode operation. The TIA stage serves as load and anti-aliasing filter for the passive mixer. The TIA is designed in such a way so that very low impedance is provided at the passive mixer output. TIA input impedance is given by

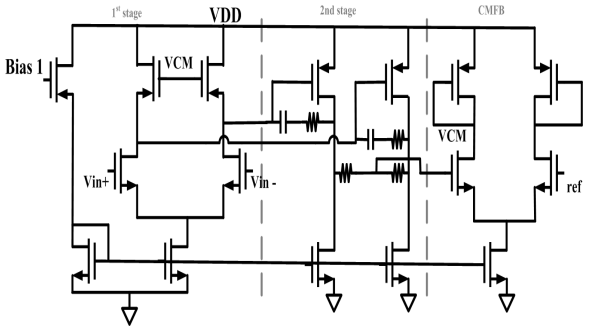


Figure 5.20: Two stage miller compensated OPAMP

$$Z_{in}(f) = \frac{2}{A(f)} * \frac{R_F}{1 + 2\Pi * R_F C_F} \tag{5.3}$$

Where A(f) is the open loop gain of the OTA. Due to high gain OTA bandwidth is limited

and high frequency components suffer high impedance. In order to filter out high frequency components C_F is inserted. This is done for all signal current to flow into feedback $R_F C_F$ from the mixer core. The Two stage opamp draws a total of 3.3mA from the supply. The gain of the TIA can be tuned by changing the value of R_F and it provides another degree of freedom to configure the gain of the downconverter.

5.4.4 Simulation Results

The RF front-end demodulator is designed and extracted in CMOS 65nm process. Post layout extracted result has been shown below. The layout area including all pads is 0.7 mm * 0.7 mm. All bias voltages are generated internally. BGR is designed to provide fixed bias regardless of temperature and supply. For incorporating the parasitics of the ESD pad, the PCB and the package bond wires into the simulation.

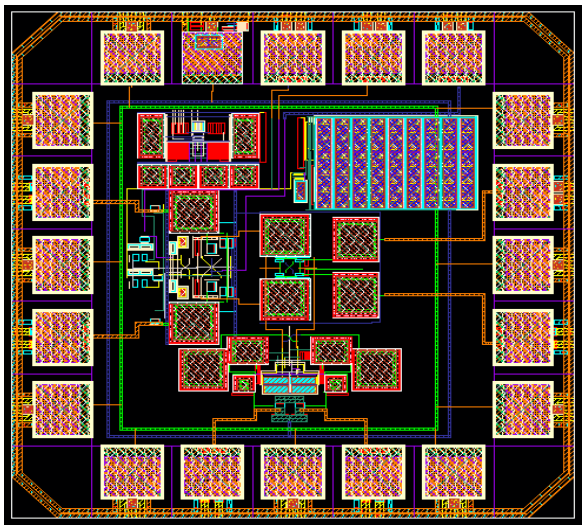
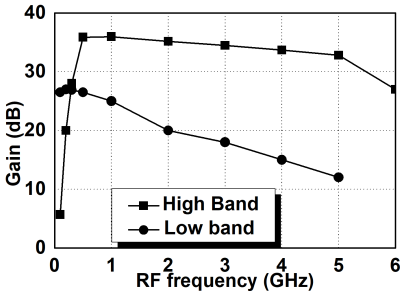
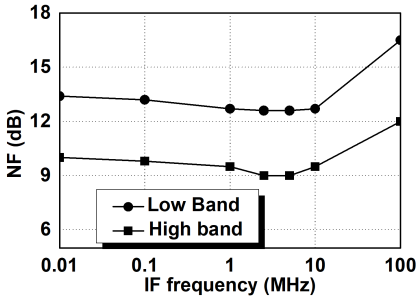


Figure 5.21: Layout of Reconfigurable Down Conversion Mixer.

The voltage conversion gain plot is shown in Fig. 5.22(a) with respect to RF frequency at 2.5 MHz IF. The voltage conversion gain is close to 27/35.4 dB for LB and HB mode respectively.

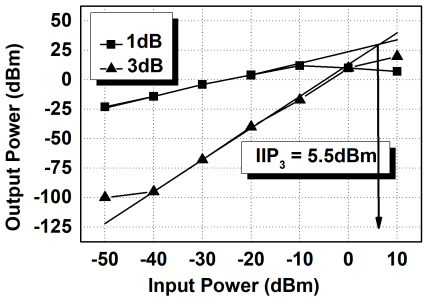


(a) Simulated conversion gain reconfigurable mixer vs RF frequency.

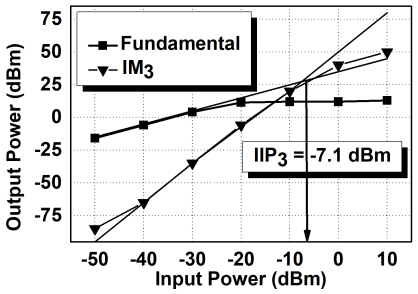


(b) Simulated noise figure vs IF frequency.

Figure 5.22: Simulated conversion gain and noise figure of reconfigurable mixer



(a) IIP_3 of HB Reconfigurable mixer.



(b) IIP_3 of LB Reconfigurable mixer.

Figure 5.23: Simulated linearity of reconfigurable mixer

The simulated double side band noise figure receiver front-end (with PSS and Pnoise analysis in SpectreRF) for an impedance matching of 50 with PCB parasitic (in SS corner) at 200MHz and 2GHz (LO frequency) for LB and HB respectively is shown in Fig. 5.22(b). The Simulated noise figure for active/passive is 12.6/9 dB for LB / HB case respectively. The two tone linearity test results are shown in Fig.9 for 2GHz and 600MHz LO frequency for HB and LB. Two tone were located at fLo + 10MHz and fLo + 25MHz. All input referred point were calculated from the input referred power and tones. Due to high conversion gain at low IF, the output compression point of the OPAMP, limits the input referred linearity of the circuit. 1dB-compression point of the circuit is limited by the output swing and varies with IF frequency. The Extracted IIP3 of HB is shown in Fig. 5.23(a) IIP3 is -7.1dBm and for LB is shown in 5.23(b) is 5.5dBm.

A Figure of Merit (FoM) given in chapter 4 suitable for evaluating the proposed reconfigurable

Table 5.4: Simulation results of Reconfigurable High/Low band Passive Down Conversion mixer for wide band Receiver and Comparison

Parameters	High band (This work)	Low band (This work)	[89]	[42]	[84]	[87]	[79]
Gain (dB)	35.4	27	19.5-21	22.5-25	35	1.2-17	3.5-20.5
NF(dB)	9	12.6	11.4-12.4	7.7-9.5	10	≥ 11	≥ 8
IIP_3(dBm)	-7.1	5.5	8-9	≥ 7	11	8.6	≤ 8.5
Power(mW)	12.48	6.3	5.4	10	20.25	5.9	5.6-9.6
BW(GHz)	.7 to 5	.1 to .7	.048-.86	1.55 to 2.3	.7 to 2.5	1 to 12	.7 to 2.3
Tech.(CMOS)	65nm	65nm	130nm	180nm	130nm	130nm	180nm
Supply	1.2	1.2	1.2	2	1.5	1.2	1.8
FoM	184.89	8.5	13.5	37.71	97.41	73.77	41.3

down conversion mixer is given in Table 5.4 and the same is calculated for the related recent works as given in Table 5.4. Reconfigurable down conversion mixer in High band has the better FOM. Thus the proposed architecture is the better solution for realization and overall FoM.

5.5 Fabrication of Wide-Band Reconfigurable (Active / Passive) Mixer

The Reconfigurable mixer circuit discussed in the section 5.2 is designed and simulated for the proof of concept and feasibility. The same is optimized here for fabrication, accounting for parasitics. In this section, design, fabrication, characterization and measurement results of a fully differential down conversion mixer have been discussed.

Full circuit description:

Design of fully differential reconfigurable (active/passive) down conversion mixer circuit is further optimized. Switches (1,2) is changed to NMOS because NMOS switch offer better speed due to its low aspect ratio (low on resistance) as compare to PMOS, as this is the signal path so PMOS switch is replaced by NMOS switch. Further TCA described in section 5.2.1 is changed to MGTR TCA explined in chapter 3. All device dimensions are given in Table.5.5, TCA dimension is given in chapter 3. The simulation of down conversion mixer is done using UMC 65nm RF CMOS technology in Cadence design environment with SpectreRF simulator. Physical verification is

done in Mentor Graphics Calibre tools. One of the major challenges in design is the layout parasitic impact in GHz frequencies. In reconfigurable circuits, the switch parasitics are an additional overhead. Each switch is optimized (between less on-resistance and less capacitance) according to their position and purpose.

The major challenge is to design a buffer which works in both modes (active/passive). A fully differential common source amplifier is added as a buffer at the output for output matching and measurement purposes. All bias voltages are internally generated for mixer biasing. ESD protection is included for all I/O interfaces. The bias generation circuit and ESD protected pads discussed in Chapter 3 are used here as well for bias generation and I/O interface. Each leg of the proposed buffer consumes 8 mA/16mA in case of passive/active respectively current from 1.2V supply.

Table 5.5: Circuit element values and transistor aspect ratio for the tapeout Reconfigurable (Active/Passive) Mixer

$(\frac{W}{L})_{M_{n1}-M_{n2}}$	$(\frac{W}{L})_{M_{n11}-M_{n22}}$	$(\frac{W}{L})_{M1-M2}$	C_c	R_F, C_F
$(\frac{42um}{600um})$	$(\frac{120um}{60um})$	$(\frac{20um}{60um})$	4pF	1.2KΩ, 5p

Impact of switch resistance on gain and noise performance:

A major difficulty in the design of a reconfigurable circuit is realization of its configuration switches. At RF frequencies, the switches along the signal path should posses less ON-resistance and less parasitic capacitance simultaneously. While the high 'ON' resistance of the switches degrades the gain and noise performance, high parasitic capacitance reduces the gain and bandwidth of the circuit. Hence, a reconfigurable circuit utilizing multiple number of switches should clearly investigate the impact of switches on its performance. However noise and gain reduction by using switch in signal path can not be canceled, but it can be minimized by proper selection of switch.

Layout Design and Optimization:

Physical implementation of this reconfigurable LNA is done in Cadence environment and verification is done using MentorGraphics-Calibre tool suite. RF MOS devices are used in whole circuit except bias and logic circuits. Resistances are realized through RNHR and Metal-Insulator-Metal (MIM) capacitors are used for DC de-coupling while MOS capacitors are used for AC-bypass. All biases are designed using same techniques as shown in chapter 3.

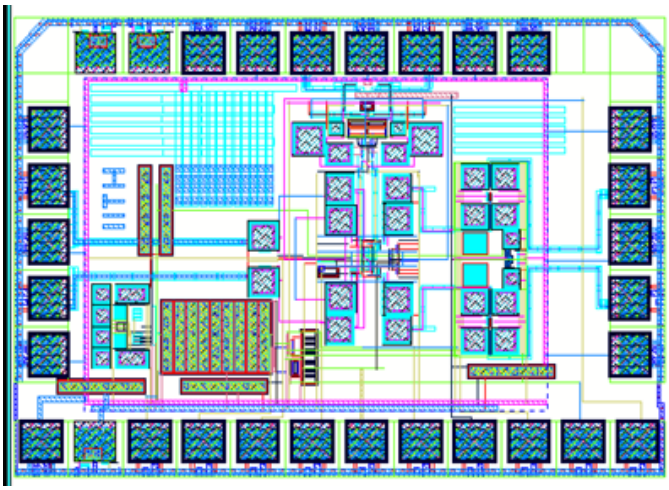


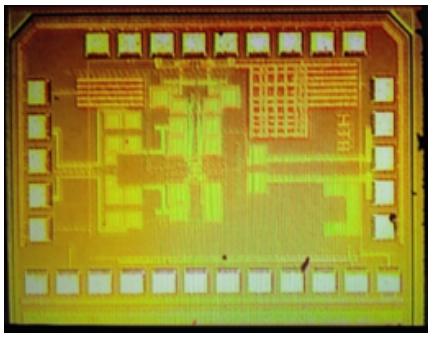
Figure 5.24: GDSII of reconfigurable down conversion mixer.

This reconfigurable down conversion mixer is implemented in UMC 65nm μm 1P9M2T1F1U RF CMOS technology. All internally generated bias voltages are terminated in pads to facilitate monitoring as well as to apply externally. All DC pads are placed with 100μm pitch while RF pads are with 100μm pitch spacing. A set of OPEN and SHORT patterns of GSG pads are also included for accurate calibration of pads. Complete circuit including pad and ESD ring occupies 1*1.2 mm^2 area. The layout diagram of the taped out (gdsII) reconfigurable down conversion mixer is shown in Fig. 5.24.

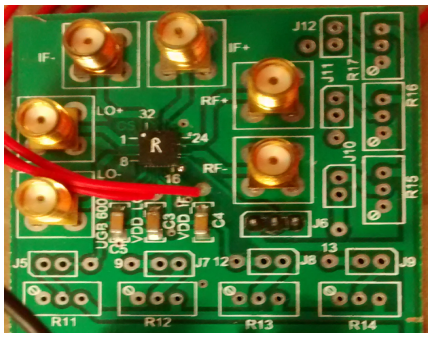
5.5.1 Measurement Result

Measurement Setup:

Fabricated die photograph of reconfigurable (active / passive) down conversion mixer is shown in Fig. 5.25(a). A customised PCB is used to generate control signals for selecting operating modes shown in Fig. 5.25(b). A 100Ω off chip resister is used for input matching. Agilent DC power supplies are used for DC characterisation. Agilent Vector Network Analyser (VNA), E8538 is used for LO generation. Rohde and Schwarz AMU200A base band signal generator is used for RF signal generation. Agilent noise figure analyser, N8975A is used for noise figure measurement and IF spectrum.



(a) Chip microphotograph of reconfigurable down conversion mixer.



(b) Assembled test board of Reconfigurable down conversion mixer.

Figure 5.25: Die photo and assembled board of Reconfigurable Mixer

Result and Discussion:

Assembled board is used for characterization of reconfigurable down conversion mixer. Test results of each mode is computed and presented here. The measured results are shown below in different operating modes.

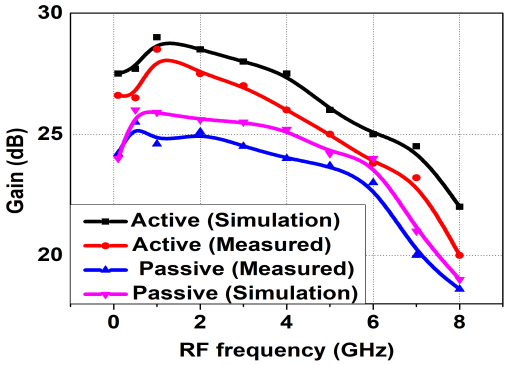


Figure 5.26: Conversion gain of reconfigurable down conversion mixer.

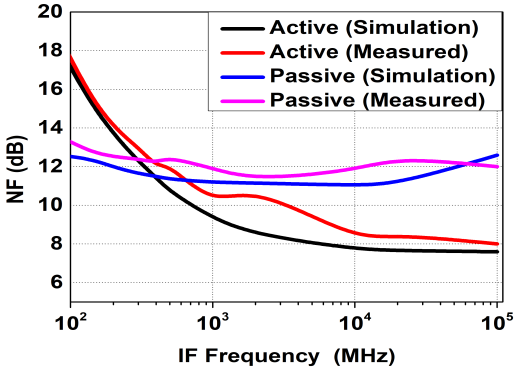
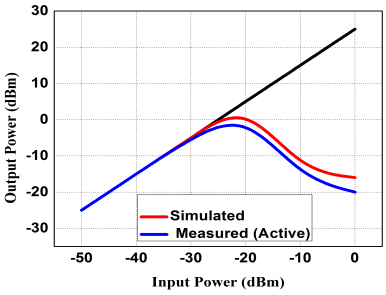
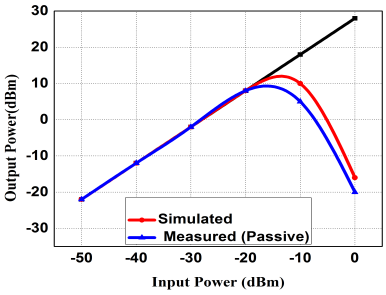


Figure 5.27: Noise Figure of reconfigurable down conversion mixer.



(a) 1dB-CP of reconfigurable down conversion mixer (Active mode).



(b) 1dB-CP of reconfigurable down conversion mixer (Passive mode).

Figure 5.28: Measured linearity of Reconfigurable down conversion Mixer

Table 5.6: Performance summary of measured results

Specification	Active	Passive
Gain (dB)	28	25
Noise figure (dB)	8.1	11.9
1dB-CP (dBm)	-20	-10
power(mW)	11.16	10.9
Bandwidth(GHz)	$1-4$GHz	$0.5-5$GHz
CMOS Technology	65nm	65nm
Power supply (V)	1.2	1.2

Fig. 5.26, Fig. 5.27 shows the measured gain and noise figure simulation vs measured of both modes (Active / passive). measured results varies around 1dB form simulation because of board paracitics and switch paracitics. Measured conversion gain shows 3 dB bandwidth from 1 to 4GHz for active case and 0.5 -5 GHz for passive case. Fig 5.27 shows the measure noise figure of both cases compared with simulation results. Fig 5.28 ahow 1dB-CP of both cases. All results are almost matching with simulation results. Fig. 5.28(a) and Fig. 5.28(b) shows the measured vs simulated linearity in active/passive case respectively. Measurement results are perfect match of simulated result. Summary of measure result is listed in Table.5.6.

5.6 Summary

This chapter has explored the techniques for integrating single hardware reconfigurable multi-mode Down conversion mixer with different reconfigurability. Component sharing is effectively utilized in between different operating modes of the proposed reconfigurable down conversion mixer to achieve good area efficiency. Methods for accounting the losses associated switches are also addressed in this chapter. Finally, a fully integrated reconfigurable multi-mode down conversion is designed, fabricated and characterized. Futher the measurement results are discussed in detail. Thus, this design proves the possible techniques for efficient design of multi-mode reconfigurable down conversion mixer.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

This thesis has introduced an approach for out of band blocker sensing using multipath scheme depicted with a major focus on the design, analysis and realization of a high performance wideband receiver architecture. An auxiliary (subthreshold) receiver is designed for out of band sensing. In main path receiver, a high gain inductive degenerative composite NMOS/PMOS transistor pair differential LNA is proposed, simulated, extracted, measured and verified analytically. This technique enhances the input matching, gain bandwidth, noise. An accurate analytical design methodology for wide band impedance matching network has developed. Further a passive down conversion mixer with improved linearity MGTR TCA and integrated baseband filter is integrated. A complete chain is extracted using post layout in 65nm technology and verified using real time measurement in CMOS process. Source follower buffer is also designed for output matching and measurement purpose. Impact of buffer on gain and noise figure is discussed. For auxiliary path a subthreshold differential receiver for out of band sensing is designed with very low power. In auxiliary path ultra low power wide band LNA and bandwidth extensive gilbert cell active mixer is proposed, designed, integrated in 180nm technology. Both simulation and measurment results are verified analytically. All integration issues are discussed and taken care of. Utilizing Further, standalone re-configurable down conversion mixers are proposed as ac-

tive/passive, low/high RF bandwidth configuarability and a comparison are drawn with previous down conversion mixers.

6.2 Future Scope

The proposed work in this thesis can be further carried out as follows:

- Design a tunable notch filter controlled by auxiliary path receiver.
- Back end correction by Digital cancellation of nonlinear out-of-band blocker distortion in wideband receivers.
- Development of suitable techniques to improve the further noise figure.
- To design wide band receiver with ultra low power.
- Design of suitable phased lock loop (including a voltage controlled oscillator(VCO)), analog-digital data converters (ADC), on-chip calibration and self-test controller block for complete receiver solution.

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