Fabrication of Hybrid Photo detector

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This thesis entitled "Fabrication of Hybrid Photo detector" by Harsha S is approved for the degree of Master of Technology from IIT Hyderabad.

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Dedicated to

My Parents

Abstract

Photo Detector is a sensor that detects light (and other Electromagnetic energies) and converts the detected energy into measureable electrical quantities with applications ranging from medical diagnosis to nuclear installations. The need for these kinds of applications is light, stable, highly sensitive sensor with a very low response time.

It is a known fact that the III-V semiconductors are being used as materials to detect photons. But with their low efficiency using III-V semiconductors as a standalone detector is not a feasible option means for further electron multiplication must be used for better efficiency. Bombardment onto silicon substrate by highly accelerated electrons can give rise to large number of electron hole pairs and further enhancement in electron number can be achieved in the avalanche region of diode thus increasing the sensitivity of the photo detector. It is also reported that the use of guard rings in Silicon avalanche diode will increase the stability of the system by creating uniform electric field throughout the device.

In this work we have simulated and fabricated a CMOS compatible Silicon Avalanche Diode with guard rings. A uniform electric field was observed in the active area of the device and the fabricated device with guard rings showed an increase in breakdown voltage when compared to the devices without guard rings thus indicating higher stability of the devices with guard rings. In addition to this the avalanche gain obtained with devices with guard rings was higher when compared to those without them. In this kind of electron bombardment system since the multiplication of electrons happen on a single substrate the response time would be less. Thus in this work we propose that the use of Silicon Avalanche diode with guard rings is more suitable in Hybrid Photo Detector for the targeted applications as the system is more stable and sensitive, fast and also light in weight.

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Chapter 1

Introduction

Photo Detector is a sensor that detects light (and other Electromagnetic energies) and converts the detected energy into characteristic electrical signals such as current and voltage. It finds interesting applications in varied fields like medical diagnosis, communication system (LIDAR) and nuclear installations. Photo Detectors are mainly classified into Photoconductive and Photo emissive types.

Photoconductors are basically Bulk semiconductors, acting as a light dependant resistors. They are based on generation of electron hole pairs in the depletion region of the junction formed. They are light, fast, compact and exhibit high quantum efficiency. The sensitivity of the device is less, and it might lead to spurious generations of current in the depletion region. The range of wavelengths that can be detected using these junctions depends on the junction depth of the device. The different kinds of photoconductors include p-n junction diodes, PIN diodes, Metal semiconductor –Metal detectors, Phototransistors , photo resistors to name a few.

Photo emissive type of photo detectors are based on principle of photo electric effect where the incident photons are converted into free electrons. Photo cathodes, photo multiplier tube (PMT), vacuum tube work on this principle. Photo cathodes are basically III-V Semiconductors which emit electrons on incident of photons. PMT's make use of secondary emission of electrons by dynodes for sensitive photon detection.

With the increasing need to increase the sensitivity of detection using a compact light weight, low cost device there is a need for a combination of photo conductor and photo emissive type of detectors. Hybrid Photo Detector is combination of a Photo cathode (Photo emissive) and a Silicon based Avalanche diode (Photo conductor) housed in a Vacuum tube.

The electrons from the photocathode are accelerated towards the diode where they undergo multiplication. The semiconductor diode serves as a dual multiplier in the system. The accelerated electrons on striking the substrate give rise to bombardment gain and further gain enhancement is achieved by the reverse biased junction of the diode. Electron Bombardment on Semiconductor Diode and avalanche multiplication in the junction region increases the overall gain of the when compared to just the secondary multiplications in Dynodes of the PMT's.[1] Since the processes are confined to a single substrate, the losses which would have otherwise occurred due to electron travelling between dynodes are minimized. This also helps in improving

the *Signal to Noise Ratio* of the system since there is no intermediate electron loss and interference due to electron transmission [5].This increases the overall sensitivity of the device thus producing more accurate results. The response time of the device is less when compared to the conventional PMT's thus making it more suitable for applications with stringent time constraints Control of electric field in the active region can lead to less dark current leading to increased sensitivity of the device. Use of a single diode in the system reduces the cost, weight. Thus it is a fast, small, low cost and a light weight device [2].

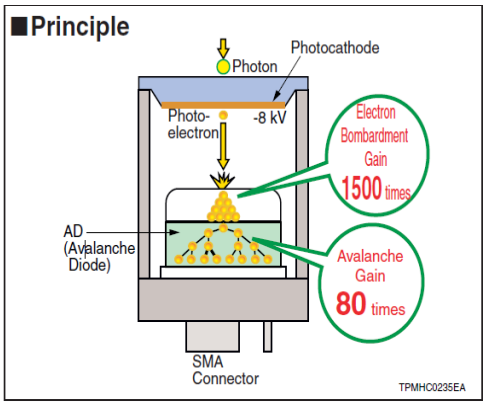


Figure 1.1 Hybrid Photo Detector [3]

Optimizations are needed towards the physical constraints for the device, placement of semiconductor diode in the tube, focusing of electrons from the photo cathode, construction of the semiconductor device for proper gain enhancement and effective collection of the electrons from the detector.

Physical constraint like temperature affects the operation of the semiconductor diode in producing the electron hole pairs. The vacuum to be maintained in the tube determines the mean free path of the electrons and this determines the optimum distance to be maintained between the semiconductor diode and photocathode and any variation in this placement can affect the sensitivity of the detector.

The Semiconductor Diode which is the source for electron multiplication has to be designed to maximize the electron gain. Proper doping profiles have to be maintained for maximum electric field in the active region to alleviate problems of dark current and early breakdown [4]. This calls for some modifications from the regular PN Diode structure. Any variations in these profiles will decrease the stability of the device which is one of the primary concerns for switching over from conventional PMT to the proposed HPD.

The proposed project involves simulation and fabrication of Silicon Avalanche Diode with guard rings using CMOS compatible process to be used as a substrate for electron bombardment

and as an Avalanche multiplier in Hybrid Photo Detector. Drift-Diffusion TCAD simulation of the device need to be carried out in order to verify the effect of Guard rings to show enhanced electric field in the bulk of the diode thus reducing the premature breakdown effects due to enhanced electric field in the corners. This involves accurate control of doping concentrations in the active region and the guard ring regions of the device. The other aspect of the project involves the fabrication of Silicon Avalanche Diode with guard rings to verify the increase in the breakdown voltage of the devices.

There are number of device structures proposed for the Silicon Avalanche Diodes with guard rings. The use of silicon avalanche diode is not restricted only to avalanche multiplication but also as a substrate for electron bombardment. Thus in addition to the structures for guard rings the structural modifications have to be made to enable electron bombardment without any barriers onto silicon substrate. The proposed device structure and other details regarding the placement of Silicon avalanche diode with respect to the III-V semiconductor photocathode and the materials for the same and other physical parameters needed for the operation of the sensor are discussed in Chapter 2 –Literature Survey of the thesis as

Drift-Diffusion TCAD simulation was carried out to verify the effect of guard rings in enhancing the electric field in the active region of the devices. The doping concentrations and the analytical profiles of the device were designed to observe the effect of guard rings as indicated discussed in the earlier section. In order to account for the various physical phenomenon involved in the device when the electron is bombarded onto the diode substrate, physical models to account for recombination generation phenomenon, mobility variations, tunneling and avalanche breakdown were included in the simulation. Sentaurus TCAD tool was used for the process [6]. The details of the parameters included in the models described above in included as a part of TCAD Simulations in Chapter 3 of the thesis.

The Fabrication of CMOS compatible Silicon Avalanche Diode is discussed under Fabrication in Chapter-4 of the thesis. The fabrication involves number of steps and the optimizations corresponding to each of them. The primary tools needed in creating the required junctions for the Silicon Avalanche Diode are the diffusion and ion implantation. The various optimizations for obtaining the desired doping concentration and the profile to match with the TCAD simulations are discussed in the chapter along with the characteristics of other process involved in the fabrication.

The results obtained for electric filed distribution which is the primary concern of the use guard rings in silicon avalanche diode are discussed and analyzed for different physical models used in TCAD simulation in Chapter-5.Silicon Avalanche Diode is characterized using Secondary Ion

Mass Spectroscopy (SIMS), Field Emission Scanning Electron Microscope (FESEM) and probe station for IV characteristics. The various characteristics of the fabricated devices including diode parameters the avalanche gain and the theoretical bombardment gain and the overall gain of the system are also discusses in the same chapter.

The conclusion of the work done in fabricating the Silicon Avalanche Diode and the enhancements needed to be done on the present work to obtain a stable, highly sensitive robust hybrid photo detector is discussed in Chapter-6 of the thesis.

Chapter 2

Literature Survey

The importance of diagnostic technique/tools like Laser Scanning Microscopy for medical imaging, LIDAR in communication systems, agriculture etc. and Nuclear reactors as source of energy and security is on the rise in present situation. One common factor in the above mentioned processes is the need for highly sensitive detectors. LIDAR requires good sensitivity for translation from Light Intensity to the distance measured and same is the case in medical imaging where 3-D images of highly sensitive internal organs are obtained. The use of sensors in nuclear reactors plays a very important role in detecting any harmful leakage from the reactors. In case of medical imaging techniques, the size of the sensor also becomes an important factor.

We need sensors that can provide all these in a single platform. The proposed HPD offers all these expected parameters from the sensor

The primary phenomenon starts with the choice of photocathode, which depends on the range of wavelength in the electromagnetic (EM) spectrum that is being targeted for detection. Indium Gallium Arsenide is used for wavelengths in the range 1.1um-1.7um and Indium Antimonide is used in the range 1um-5um.

Table-2.1: Material of photocathode and the corresponding region of detection in EM spectrum [1]

Photocathode material	Targeted Region
Bialkali Photocathode	Visible
Multialkali Photocathode	IR
Alkali Halides	UV

The system must be housed in a vacuum of around 10^{-4}Pa [1].This pressure condition will lead to the calculation of the optimum distance between the photocathode and the semiconductor diode. The mean free path of electrons 6.6mm at the given vacuum level will be the optimum distance.

The quantum efficiency of the photocathode being used also depends on the wavelength being detected [6]. Appropriate doping makes the cathode more electropositive thus increasing its Quantum Efficiency. This process is called Photocathode activation.

The main focus in the present proposal is the work on semiconductor diode. The primary purpose of using the diode is for electron bombardment. In silicon an electron hole pair is

created every 3.6ev of incident energy [14]. The bombardment gain also depends on the acceleration of the electrons from the photocathode as indicated in Fig 2.1 [1, 2, 5,7,8] and also on the threshold energy for bombardment, which in turn depends on the thickness of Dead space of the diode, which the electrons from the photocathode have to penetrate in order to reach the active area [8,9]. The energy lost in the dead layer(Metal Contact) depends on the stopping power of the given material for the given incident energy [15]. The stopping power for aluminum for different incident energy of electrons is given below in Table 2

Table-2.2: The stopping power for aluminum for different incident energy of electrons [15]

Incident Electron Energy(KeV)	Stopping Power(eV/A^0)
1	2.44
2	1.64
4	0.998
6	0.736
8	0.590
10	0.495

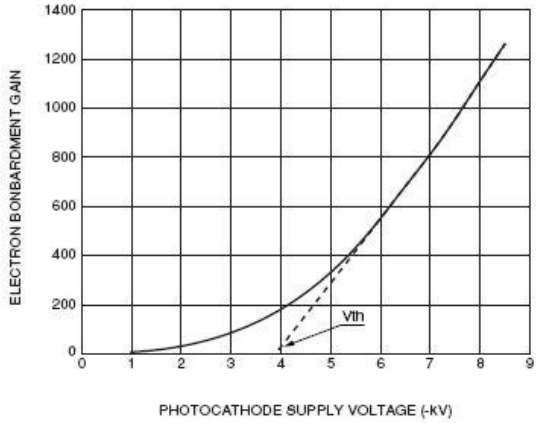


Figure 2.1: Variation of Bombardment gain with Photocathode supply voltage [1]

The use of diode in avalanche region gives more control over the gain by adjusting the avalanche bias voltage as indicated in Fig 2.2 Thus the device offers more tunability than the conventional PMT's.

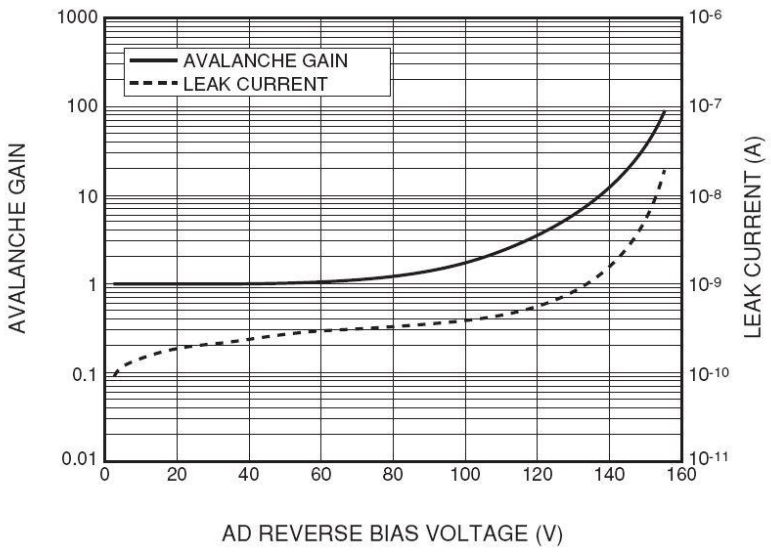


Figure 2.2: Variation of Avalanche gain with Avalanche diode biasing [1]

Avalanche breakdown occurs when there is a wide space charge region. If the width is wide enough such that it is greater than the mean free path of electrons between collisions multiplication of charge carriers takes place leading to electrical breakdown. A p+-p-n+ structure is suitable for desired results as it gives rise to wide space charge region as indicated in Fig 2.3 producing enough space for the bombardment generated electrons to drift through to the avalanche region for further amplification. In addition to the n+ layer, diffused guard rings (n regions adjacent to the n+ regions) are essential for enhancing the electric field at the active regions of the device thus preventing premature edge breakdown [4]

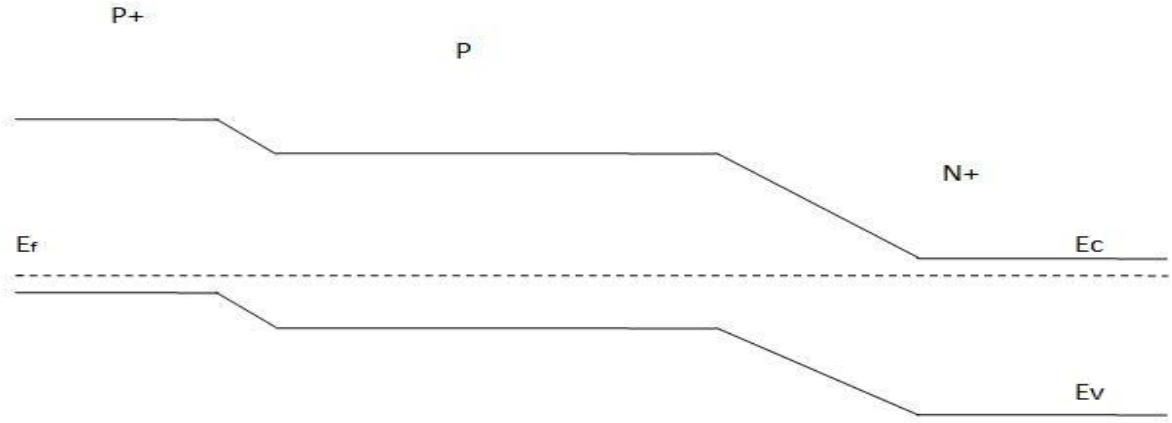


Figure 2.3: Band Diagram of P+-P-N+ structure

There have been various designs proposed for the guard ring structures. Use of retrograde doping profile to get a virtual guard ring kind of structure was proposed by Tomer Leitner et al., in [10].This requires accurate control of doping in vertical direction. Jusitn A Richardson et al. proposed a deep N-well p–well guard ring structure [11] similar to the one proposed by Kamrani et al. in [4].They also proposed an n-enhancement region in deep n-well process which also acts as an virtual guard ring by enhancing the electric field in the active region of the device.

Pancheri et al. in [12] proposed the use of both the enhancement region as well as p-well region in an epitaxially grown layer of doped silicon. Similar structures with epitaxial grown layer have been proposed in [13] and [14] by Lin Qi et al.

The main motive behind the use of these structures is the reduction in the electric field at the corners that can be obtained. Different structures proposed have their significance in different technology nodes that they can be implemented in. The best structure is to be chosen based on the available fabrication facilities.

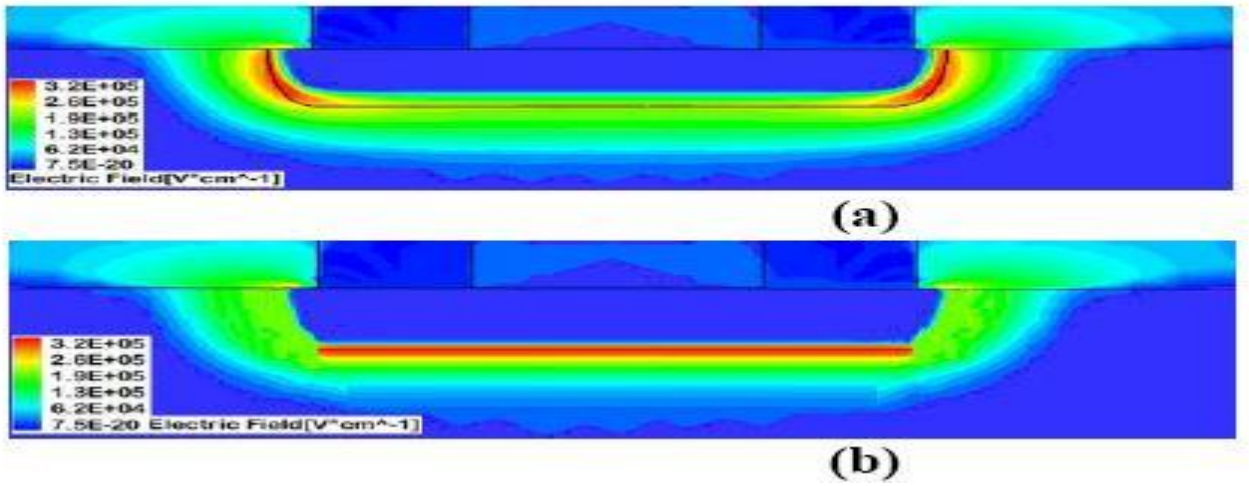


Figure 2.4: a) Avalanche Diode without Guard ring b) Avalanche diode with guard ring [4]

The P+ region will be facing the photocathode. The Ohmic Contact between the p+ region and the metal contact (anode) will let electrons bombard on the device to produce electron hole pair.

From the Band diagram in fig 4.2, it is obvious that there is no barrier for electron transport from metal to semiconductor because of the Ohmic contact and with the energy gained by these electrons due to the accelerating potential applied at the photocathode, they produce electron

hole pairs. The main reason for this is the reduced barrier height which can be increased by increasing the doping of the P+ region.

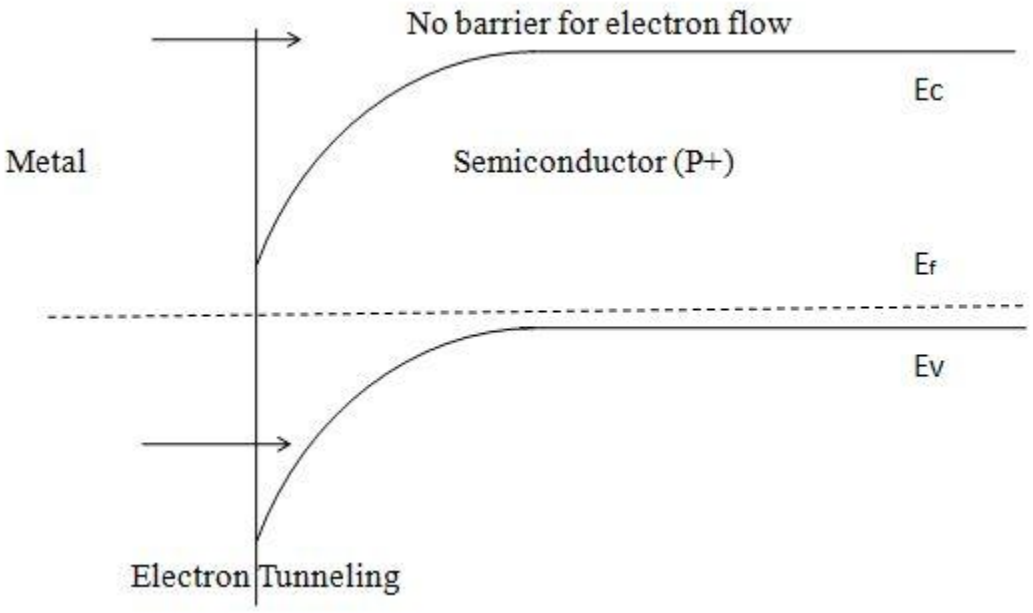


Figure 2.5: Band Diagram indicating Ohmic Contact at Metal Semiconductor Interface

The Bombardment gain depends on the energy of electron that impinges on the semiconductor region. This is given by the relation

$G_{Bombardment}=(V_{Photocathode}-V_{Threshold})$ /3.6ev [2].

Where $V_{Photocathode}$is the voltage applied to the photocathode $V_{Threshold}$ is the amount of energy lost during electron penetration through the metal [7]. 3.6ev is the amount of energy required for electron hole pair generation [13].

The electrons generated from the bombardment drifts towards the reverse biased junction. Here the second multiplication takes place with the gain achieved from it being G_A. The total gain from both the process combined together would be G_A*G_Q.

The important aspect here is the control of the breakdown voltage. The electric field at the edges of the doped region is high due to the gradation in the doping concentrations we obtain. So there is a need to avoid this. This can be done by introducing lightly doped diffused regions at the doping edges as shown in fig 4.1. This region can also suffer from the premature breakdown but the electric field at the edges but the doping concentration is less in these regions compared to the bulk regions. Thus the premature edge breakdown at the bulk regions

is avoided reducing the dark current that could have been triggered by high electric fields at the edges. The deign needs careful considerations in terms of the doping concentrations of the N and N+ regions and the positions of the positions of N regions.

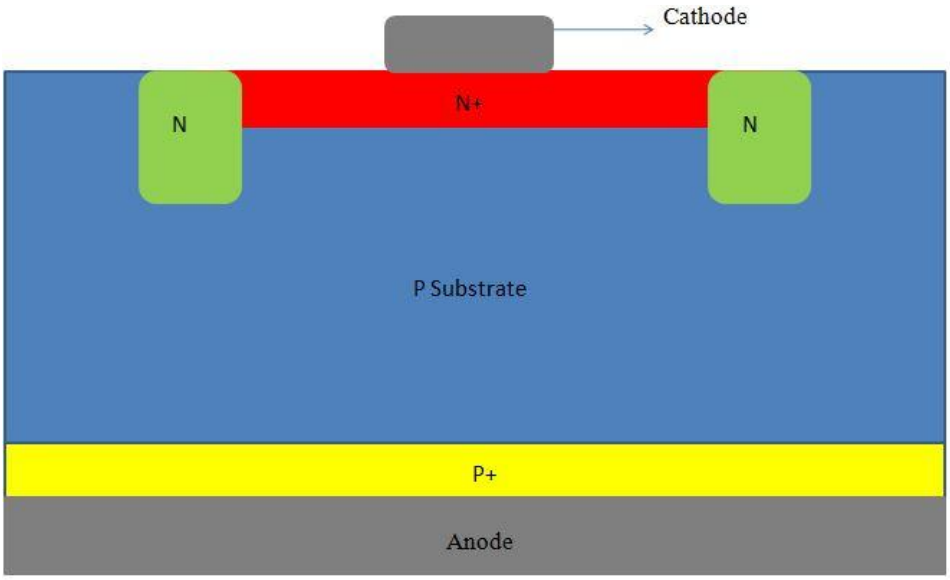


Figure 2.6: Proposed Device structure

Chapter 3

TCAD Simulation Studies

Fabricating a semiconductor device involves a lot of steps. The unique include lithography, etching, doping to name a few. These process are time consuming and not easily predictable in their effects. Technology Computer Aided Design (TCAD) is computer aided simulation tool that helps in optimizing the semiconductor fabrication process. As the proposed structure involves number of optimizations in terms of doping concentrations, position of different regions it was necessary to simulate the desired structure for optimum results. SYNOPSYS TCAD tool Sentaurus was used for the process. Sentaurus involves number of modules like SDE for structural simulations, Sprocess for process flow optimizations, Sdevice for characterization, Smesh for creating the mesh necessary for solving the equations at different points in the structure and Svisual for visual analysis for the simulated data.

3.1 Structural and Device Simulation

Structural simulation involves defining the regions with the desired profile and the concentrations. The regions in the proposed structure involve lightly doped distributed regions and highly doped steep regions. The main doping systems available are Diffusion and Ion implantation systems. The samples Ion Implanted must be annealed at high temperature to make them electrically active. The high temperature annealing gives rise to a Gaussian profile. Diffusion from a solid source also gives rise to Gaussian profile. Thus while defining the doped regions the Gaussian definition for the profile was defined. The position and the Gaussian profile variation in the N+ active region and the N guard ring regions is crucial to reduce premature edge breakdown effect.

Numbers of trails were done with different doping concentrations, positions and the Gaussian profile variations. It was observed that a doping concentration difference of about 3 orders was needed for the effect of the guard rings to be seen.

The process involved in TCAD simulation is as indicated in Fig 3.1

Figure 3.1: Process flow for TCAD Simulation

The parameters used in the Structural definition of the device are as in Table 3.1

Table 3.1: Dimensions of different regions of proposed structure

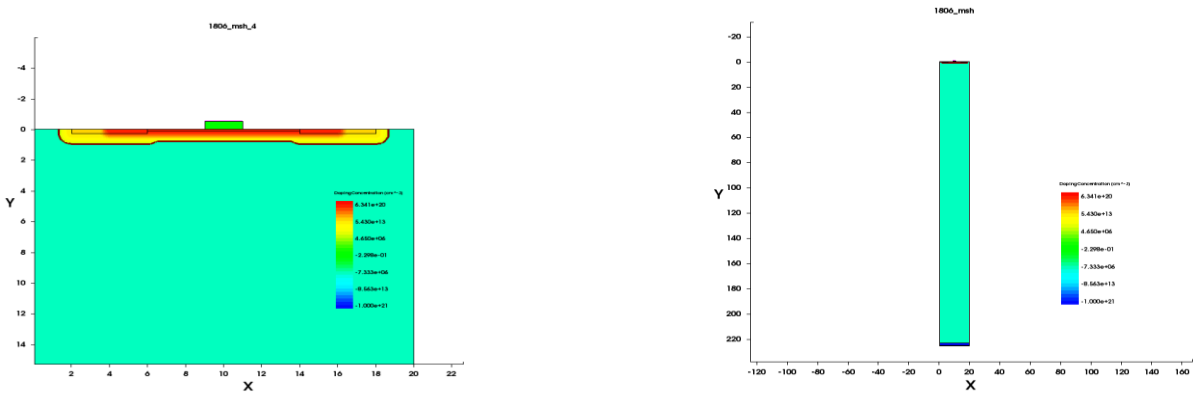
Region	Dimension(um)
N+	12x4
N	4x4
Cathode	6x4
P+	20x4
Anode	20x4

The doping concentration and the profile used for different regions of proposed device is indicted in Table 3.2

Table 3.2: Doping concentration and profile of different regions of proposed structure

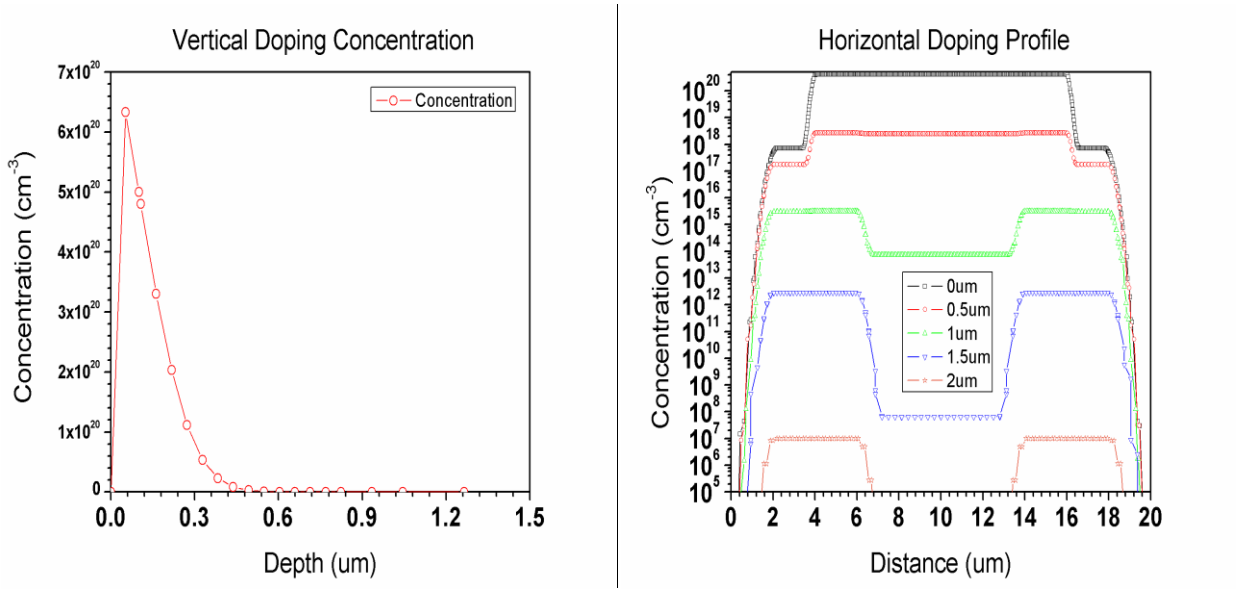
Region	Concentration (cm^{-3})	Profile
N+	$1x10^{21}$	Gaussian
N	$1x10^{18}$	Gaussian
P	$1x10^{16}$	Uniform
P+	$1x10^{21}$	Uniform

Meshing strategy with minimum mesh size of 0.1 um was used in the process. 49643 vertices were generated at the bulk of the device and 2400 vertices at the boundary regions with total mesh generation time of 41.1 s.



(a) **(b)**

Figure 3.2: a) Structure used in simulation indicating presence of Guard rings b)Figure indicating utilization of both sides of wafer for simulation



(a) (b)

Figure 3.3: a) Vertical Doping profile of the device b) Doping concentration in horizontal directions at different depths

Doping profile variation along the vertical directions shows the profile with Gaussian distribution. From the figure the effect of N regions becomes more visible towards the junction which is the necessary part for the effect of guard ring to be seen

When the electrons enter the Avalanche diode they undergo a number of physical phenomenon. The electrons undergo recombination and generation by SRH and Auger process. There is also possibility electron tunneling happening between doped regions of different concentrations. The Fermi level depends on the temperature of the device which in turn affects the intrinsic carrier density of the device. The diode contains regions of different concentrations, mobility of the electrons and holes depend on the doping concentration at the point of interest in the device. The inbuilt electric field of the device depends on the doping profile which in turn affects the mobility.

To get the accurate predictions of all these phenomenon mathematical models relating to all these combinations have to be included in simulation. In SYNOPSYS tool a number of models are present which can accurately model the physical phenomenon. The models used for simulation are described below.

3.1.1 Schokley-Read-Hall (SRH) Recombination

SRH recombination refers to recombination of electron hole pairs in deep-level-traps. Recombination rate is given by

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \quad \text{.....} \quad (3.1.1.1) \quad [6]$$

With : $$n_1 = n_{i,eff}\, e^{\frac{E_{trap}}{KT}} \quad \text{.....} \quad (3.1.1.2) \quad [6]$$

And : $$p_1 = n_{i,eff}\, e^{\frac{-E_{trap}}{KT}} \quad \text{.....} \quad (3.1.1.3) \quad [6]$$

E_{trap} is the energy difference between the defect level and the intrinsic level.

The minority carrier lifetime depends on the doping concentration [16-19]. Accordingly the carrier lifetime is given by Scharfetter relation:

$$\tau_{dop}\left(N_{A,0} + N_{D,0}\right) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^{\gamma}} \quad \text{.....} \quad (3.1.1.4) \quad [6]$$

SRH rate also dependence on the temperature of the device, but during simulation the temperature is assumed to be constant at 300k so the dependence is not considered. According to Schenk in [20], the carrier lifetime also depends on the electric field along a particular path the carrier travels. Since the proposed device is proposed to have high electric field in the active region the field dependence on the carrier lifetime is to be considered for effective modeling

Table 3.3: Default SRH Parameters [6]

Symbol	Parameter name	Electrons	Holes	Units
$\boldsymbol{\tau_{min}}$	taumin	0	0	s
$\boldsymbol{\tau_{max}}$	Taumax	$1x10^{-5}$	$3x10^{-6}$	s
$\boldsymbol{N_{ref}}$	Nref	$1x10^{16}$	$1x10^{16}$	cm^{-3}
$\boldsymbol{\gamma}$	gamma	1	1	1
T_{α}	Talpha	-1.5	-1.5	1
C	Tcoeff	2.55	2.55	1
E_{trap}	Etrap	0	0	eV

3.1.2 Auger Recombination and Generation

Auger recombination involves recombination of electron hole pair with generation of an additional electron. These help in generation of additional electrons which increases the effective current in the system. Auger recombination generation becomes more important in devices having high carrier densities The model used in the Sdevice is given by

$$R_{net}^{A} = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right) \quad \text{.....(3.1.2.1)} \qquad [6]$$

Where C_n and C_p are temperature dependant Auger coefficients increasing from 3.0×10^{-31} to 4.6×10^{-31} cm^6s^{-1} in the temperature interval 195–372 K [21]

3.1.3 Mobility Models.

Mobility of an electron infuences the effective current generated in a semiconductor device. In sentaurus Mobility variation due to phonon scattering can be considered, at varying temperatures. But since the lattice temperature is considered to be constant throught the simulation, this model is not considered.

It is known that the mobility of electrons and holes depend on the the mean collison time of the carriers. With doping the sacttering of the carriers increase thus decreasing the mean collision time. This degrades the mobility of the charge carriers. In Sdevice this phenomenon can be modeled by using Doping Dependant Mobility model. The default model for doped silicon available is Masseti model [22] given by

$$u_{dop} = u_{min\,1} e^{-\left(\frac{P_e}{N_{A,0}+N_{D,0}}\right)} + \frac{u_{const} - u_{min\,2}}{1+\left(\left(N_{A,0}+N_{D,0}\right)/C_r\right)^{\alpha}} - \frac{u_1}{1+\left(\left(N_{A,0}+N_{D,0}\right)/C_r\right)^{-\beta}} \quad \text{..... 3.1.3.1} \qquad [6]$$

The default parametes used in the models are

Table 3.4: Default Parameters of Masetti Model [6]

Symbol	Parameter name	Electrons	Holes	Units
u_{min1}	mumin1	52.2	44.9	cm^2/Vs
u_{min2}	mumin12	52.2	0	cm^2/Vs
u_1	uu1	43.4	29	cm^2/Vs
P_c	pc	0	$9.23x10^{16}$	cm^{-3}
C_r	cr	$9.68x10^{16}$	$2.23x10^{16}$	cm^{-3}
C_s	cs	$3.43x10^{20}$	$6.10x10^{20}$	cm^{-3}
α	alpha	0.680	0.719	1
β	beta	2.0	2.0	1

The velocity of the electrons saturate at high fields. Thus the corresponding increase in mobility is not observed according to the relation. Since the device considered in the simulation has high electic field in the active region this effect has to be modeled. There are models available in sentaurus that can accurately take into effect these physical phenomenon. The Models available are velocity saturation model and the driving force model. The driving force model considers the gradient of the electric field in the direction of electron travel, or the electic field normal to the point of calculation also can be considered.

3.1.4 Band Structure

In heavily doped device the effective bandgap of the semiconductor reduces due to overlap of the impurity states. Thus this effect has to be considered as it effects most of the physical phenomenon in a semiconductor device including the effective intrinsic concentrations of electrons and holes in the device. The oldslotboom model available in sentaurus is based on the n-p-n transistors model and is used devices where junction effects have to be considered [23]. The change in the bandgap is modeled using the relation

$$\triangle E_g^0 = E_{ref} \left[ln\left(—\right) + \sqrt{\left(ln\left(\frac{N_{tot}}{N}\right)\right)^2 + 0.5} \right] \quad \text{..... 3.1.4.1 [6]}$$

with the default parameters given by

Table 3.5: Default Parameters for oldslotboom Model [6]

Symbol	Value	unit
E_{ref}	$9x10^{-3}$	eV
N_{ref}	$1x10^{17}$	cm^{-3}

3.1.5 Avalanche Generation

As discussed in literature review, the structure being operated in the reverse biased mode has a wide space charge region. Thus the possibility of the avalanche breakdown has to be considered. The avalanche breakdown mechanism ia an imporatant phenomenon of the considered device, so modelling the mechanism is very important.

The general generation factor of electrons and holes is given by,

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \quad \text{.....3.1.5.1 [6]}$$

Where alpha represents the ionization coefficient of electrons and holes. V represents the velocity of electrons and holes. There are the different factors on which these co efficients depend and have to be considered for effective modelling of the physical phenomenon.

There are number of models available to model the avalanche breakdown in Sdevice.

The Van-Overstraeten model includes the Temperature dependancy of phonon velocity[25].University of Bologna Impact Ionization Model includes the temperature dependance of ionization coefficient.Hatakeyama model is used for Power devices[6]. The Okuto-Crowell model includes the temperature,position,doping concentration and the elctric field dependance on the ionization coefficient [25]. The Lackner model in addition to the dependancy included in the Okuto-Crowell model includes the path length travelled by the carriers in the device [26]. The device being simulated is assumed to be at a constant temperature, hence only field dependance on the ionization coefficients is considered using Okuto-Crowell model and the path length dependance included using the Lackner model.

3.1.5.1 Okuto-Crowell Model

The ionization coefficient is defined by the following in this model.

$$\alpha(F_{ava}) = \alpha.\left(1 + c(T - T_0)\right)F_{ava}^{\gamma}\, e^{\left[-(b[1+d(T-T_o)])^{\gamma/F_{ava}}\right]} \quad \text{.....3.1.5.1.2 [6]}$$

The coefficients b is dependant on the bandgap and the electric filed. The coefficient a dependance of the voltage drop in the depletion regions of the device. The temperature depenadance is also included in the expression, but in this simulation we are considering a constant lattice temperature, so the effect is not considered in calculating the avalanche breakdown voltage. The Default parameters used in the model are

Table 3.6: Default Parameters for Okuto Crowell Model [6]

Symbol	Parameter name	Electrons	Holes	Units
a	a	0.426	0.243	V^{-1}
b	b	4.81×10^{5}	6.53×10^{5}	V/cm
c	c	3.05×10^{-4}	5.35×10^{-4}	K^{-1}
d	d	6.86×10^{-4}	5.67×10^{-4}	K^{-1}
γ	gamma	1	1	1
δ	delta	2	2	1
λ	lambda	68×10^{-8}	45×10^{-8}	cm
β	beta	0.265283	0.261395	1

3.1.5.2 Lackner Model

This model is an modification to the chynoweth law for breakdown voltage dependance. In this model the the correction factors used were different for high and low field domains. In this model correction factors used are electric fields raning from a $1x10^5$ v/cm to $1x10^6$ v/cm. The ionization coefficent is given by

$$\alpha(F_{ava}) = \frac{\gamma a_v}{Z} e^{-(\frac{\gamma b_v}{F_{ava}})} \quad \text{where } v=n,p \quad \text{..... 3.1.5.2.1 [6]}$$

All the actors considered in Okuto-crowell model are considered here also. In addition to it the distance travelled by the electrons and holes before collision is considered and also the change in energy due to collision is considered for modeling the fitting parameters in calculating the avalanche breakdown voltage. The default parametes considered in the moodels are

Table 3.7: Default Parameters for Lackner Model [6]

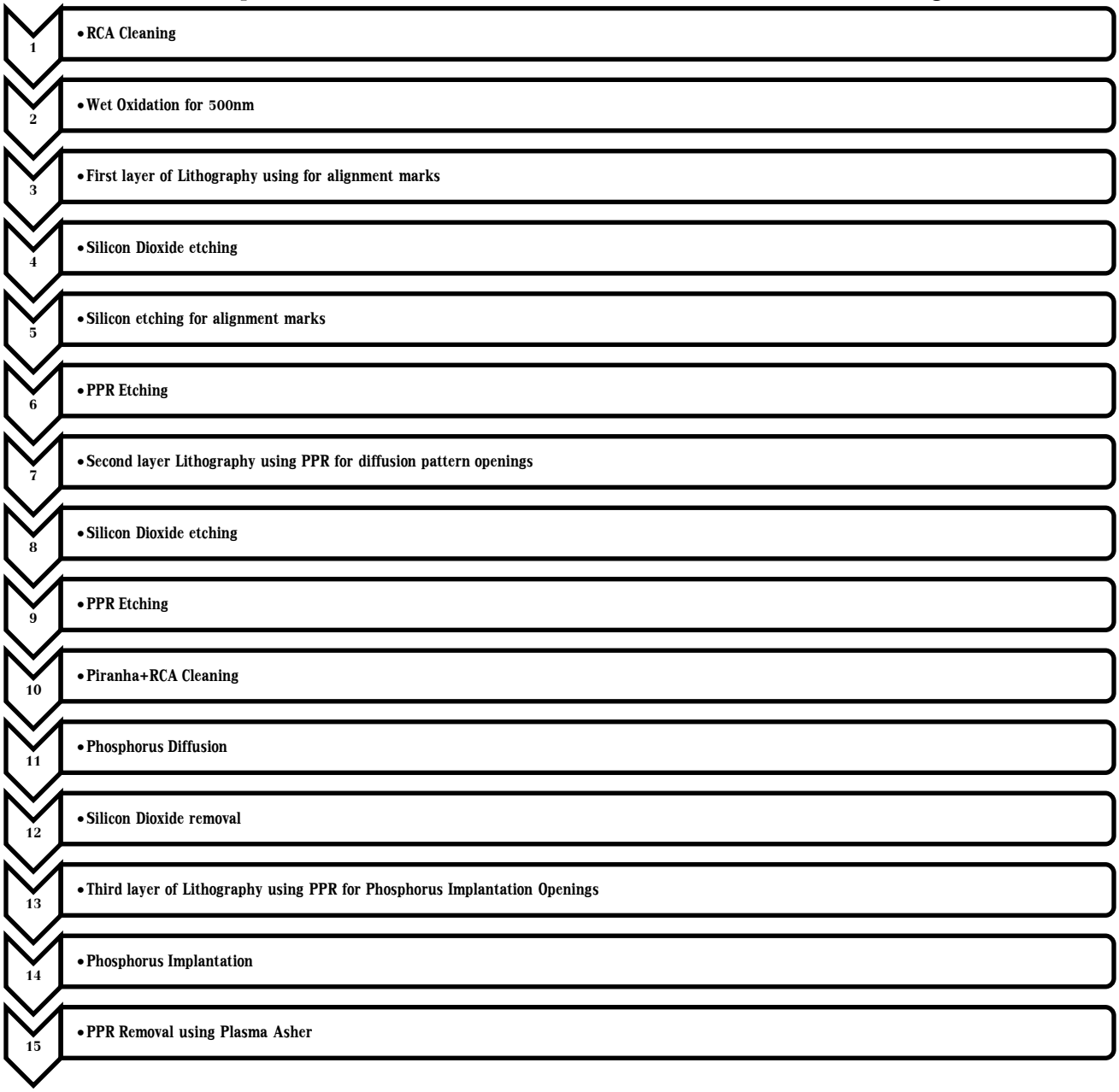
Symbol	Parameter name	Electrons	Holes	Units
a	a	1.316×10^6	1.818×10^6	V^{-1}
b	b	1.474×10^6	2.036×10^6	V/cm
$\hbar w_{op}$	hbaromega	0.063	0.063	eV
λ	lambda	62×10^{-8}	45×10^{-8}	cm
β	beta	0.812945	0.815009	1

In addition to this in all these models the electric field dependnace can be considered either at a point specified using Eparallel syntax or the gradient of electric field along the path of electron

Chapter 4

Silicon Avalanche Diode Fabrication

The device fabrication involves a number of steps. It starts with the kind of wafer needed to start the process. There are number of parameters that have to be optimized in order to get the proper device properties. The flow chart indicating the device fabrication is shown below and each of the steps will be discussed in detail in the following sections.



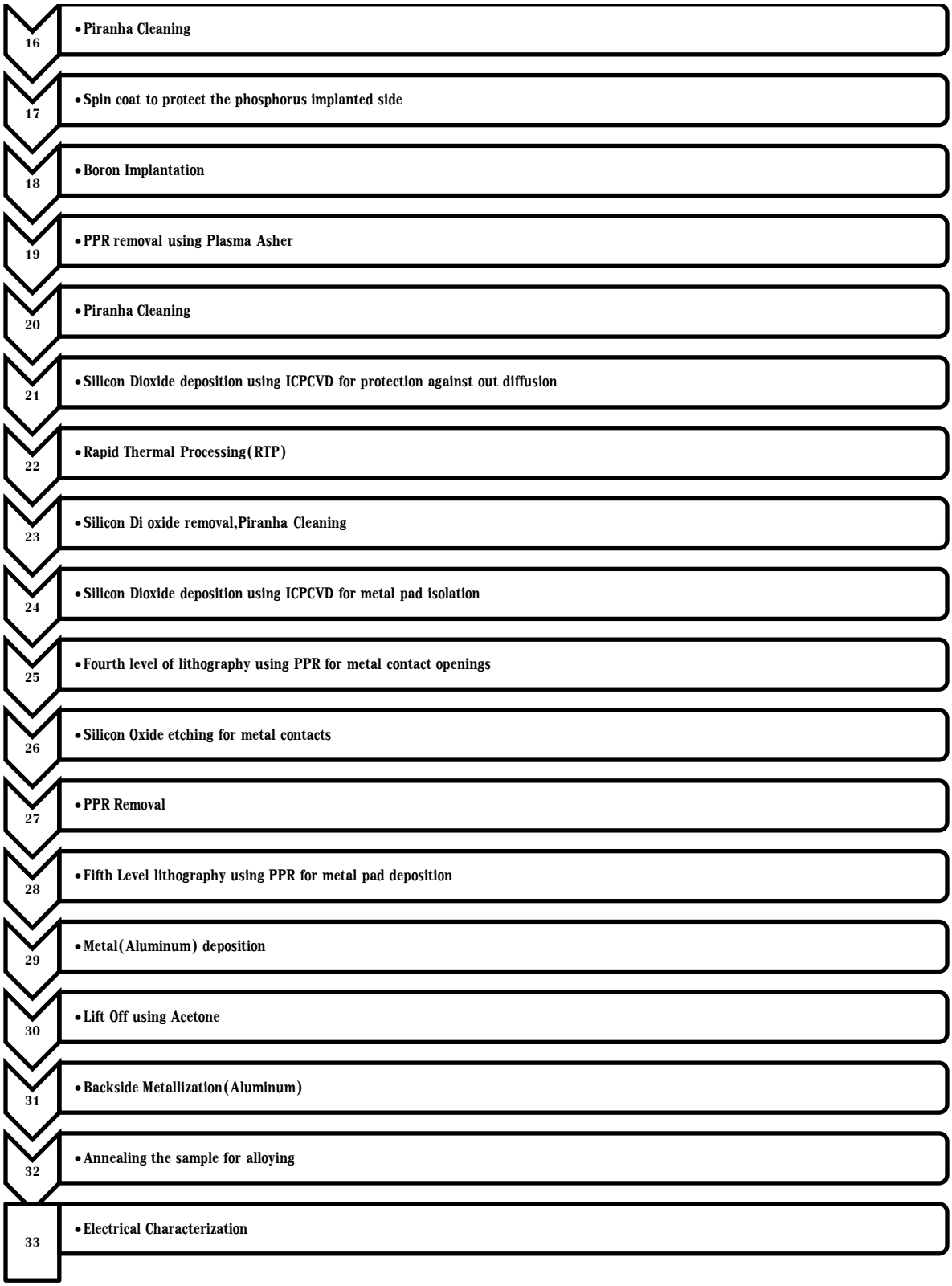


Figure 4.1: Fabrication Process flow

All the above process was carried out in CEN IIT Bombay under Indian Nanoelectronics User Program (INUP).

4.1 Wafer Specification

The process was started with 4-7 Ohm-cm, <100>P-Type double side polished Silicon wafer. This corresponds to doping concentration in the range $1.9x10^{15}$ – $3.38x10^{15}$ cm^{-3}. The wafer specification was closer to the background doping $1x10^{15}$ cm^{-3} concentration used in simulation.

4.2 RCA Cleaning

RCA (Radio Corporation of America) cleaning is the standard cleaning procedure for Silicon wafers [27]. DI water with resistivity 18 M Ohm –cm is used in the process. This is a two step procedure and is discussed below.

The process is started with a dip for 30s in 2% Hydrofluoric (HF) acid. It is used to remove any native oxide present on the wafer.

4.2.1 RCA I

RCA I is used for removing any organic and particle contaminants in the wafer. The process is as below

- Recipe: DI Water (180 ml), 30% H_2O_2 (Hydrogen Peroxide)(50 ml),29% Ammonium Hydroxide(NH_4OH)(25 ml).
- Heat mixture of DI Water and NH_4OH for 5 min at 80^0C.
- Add H_2O_2 to the above mixture and heat at 80^0C for 8 min.
- Cool the mixture for 12 min

The mixture of base –peroxide removes the organic contaminants and the particle contaminants are removed by repulsion.

The wafers are again dipped in 2% HF for 30s , to remove native Oxide.

4.2. 2 RCA II

RCA I is used for removing any metallic contaminants in the wafer. The process is as below

- Recipe: DI Water (180 ml) , 30% H_2O_2 (50 ml),Conc.Hydrochloric acid (HCl)(25 ml).
- Heat mixture of DI Water and NH_4OH for 5 min at 80^0C.
- Add H_2O_2 to the above mixture and heat at 80^0C for 8 min.

- Cool the mixture for 12 min

HCl present in the mixture forms chloride with metallic contaminants and precipitates out. This is followed by 30s dip in 2% HF.

The wafers are then dried in dry Nitrogen.

4.3 Thermal Oxidation

Silicon Dioxide is one of the major layers in silicon fabrication. There are two types of oxidation which can be used to get the oxide. Dry oxidation is process when oxide is formed on the silicon surface by reaction of silicon with oxygen directly given by

$$Si + O_2 \rightarrow SiO_2 \quad \text{..... 4.3.1 [27]}$$

This type of oxidation gives a pure oxide since there are no residues formed. The thickness obtained by this type of model is less, because of the saturation for the reaction between oxygen and silicon. This type of oxide is used when the oxide plays a very important role is determining the characteristics of the device like MOSFET.

In wet Oxidation the oxide layer is formed by the reaction of silicon with water vapors given by

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad \text{..... 4.3.2 [27]}$$

As seen in the reaction there is residual Hydrogen gas makes the oxide more porous thus reducing its quality when compared to the dry oxide. Because of the porosity the thickness of oxide that can be grown over the sample is quiet high. This kind oxide is generally preferred for usage when the oxide layer is being used as a sacrificial layer.

For the fabrication of the proposed device, oxide is used as a mask for diffusion and Ion Implantation process. They require thickness of around 400nm-500nm for effectively acting as a mask. Thus we need to go in for wet oxidation to get the desired thickness of the oxide layer.

Wet Oxidation was done using 2 inch wet oxidation furnace to have a thickness of about 500nm using pre optimized process parameters. The procedure for the same is indicated below.

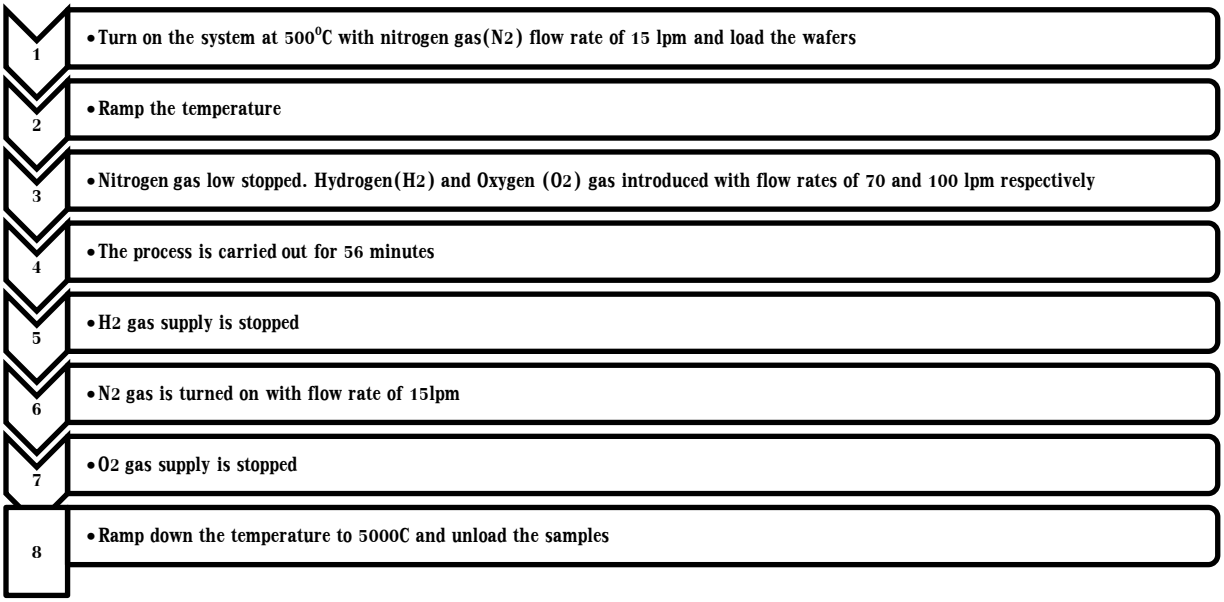


Figure 4.2: Process flow for wet Oxidation

4.4 Lithography

One of the major steps in the fabrication flow is lithography. The patterning for active device area formation is done in this step. UV photolithography is used for the purpose. Wavelength in the range 450nm-550nm is used. Positive photoresist S1813 is used throughout the process. The general procedure followed during the process is described below

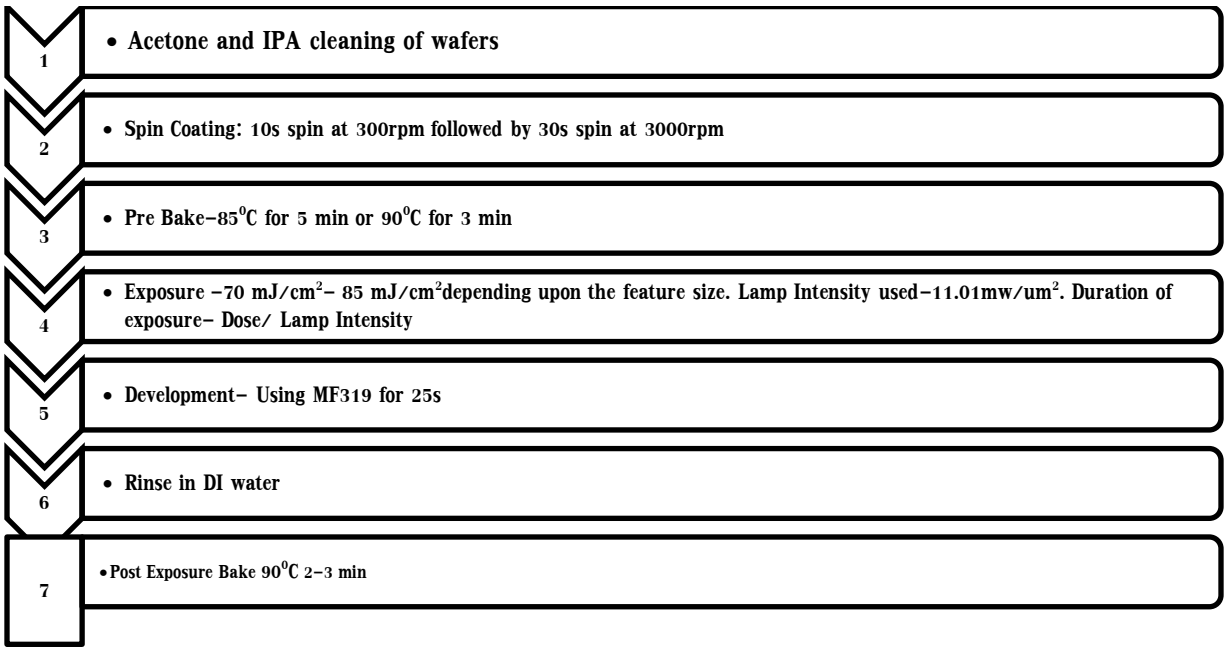


Figure 4.3: Process flow for Lithography

Karl suss Lithography system MJB4 was used for the first layer of alignment mark etching. Subsequent alignment and exposure for different layers was done using Double Side Aligner (DSA) lithography instrument.

4.5 Silicon Dioxide etching

Silicon Dioxide etching is usually done using Buffered oxide etchant. Buffered oxide etch (5:1) with etch rate of 100nm/min is used in the process. It is used for etching out oxide for active device openings and also for complete removal of oxide from the surface of silicon. PPR S1813 is used as mask for oxides etch.

4.6 Silicon Etching

The proposed device has many processes and requires proper alignment at each step. Thus Silicon is etched at certain places with etch depth around 1-1.3um. STSRIE is used to etch silicon. PPR acts as mask for Si etching. RF Plasma of CF_4 with flow rate of 40sccm for 7min at RF Power of 100w and a chamber pressure of 50mtorr was used during the process

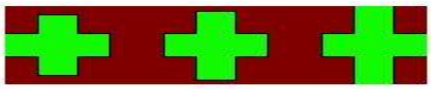


Figure 4.4: Alignment marks used during fabrication

Alignment between different layers is shown in the Fig 4.4.

4.7 Resist Removal

The resist S1813 is remove using acetone and a clean with Isopropyl alcohol (IPA) is needed for cleaning the stains left behind on the wafer by acetone.

Resist which was used as mask for Ion implantation was hardened and couldn't be etched out by acetone. Plasma Asher was used to remove the resist using oxygen plasma. The general etch rate of the system is around 250nm/min at 25sccm oxygen flow at an RF power of 100W. Since the resist used for hardened on Plasma exposure 17 minutes exposure in steps of 4 min, 8 min and 5 min was used for the complete removal of the PPR from the wafer

4.8 Piranha Cleaning

Piranha Cleaning is used to clean organic residues on the substrate. It is a mixture of Conc. Sulfuric acid and Hydrogen peroxide(H_2O_2) in the ratio 7:3 for 15 minutes followed by a 30s dip in 2% BHF for native oxide removal.

4.9 Diffusion

Introduction of dopants into semiconductor substrate is important to form junction and to explore its properties. Diffusion is movement of particles from higher concentration to lower concentration. This is according to fick's law which relates the particle flux, the diffusivity and the concentration gradient along the boundary

$$F = -D\frac{\partial C}{\partial x} \quad \text{..... 4.9.1 [27]}$$

The dopants introduced take different distributions depending upon the source used for the process. The concentration depends on the initial pre deposition step used. The depth and the profile distribution depends on the amount of time the drive in step is performed. If a finite source of dopants at the surface is used then the distribution obtained is a Gaussian profile with the distribution

$$C(x,t) = \frac{Qe^{-\frac{x^2}{4Dt}}}{(\Pi Dt)^{\frac{1}{2}}} \quad \text{..... 4.9.2 [27]}$$

Where the dose Q is determined by the initial pre deposition step.

If we have a source with a constant surface concentration then an error unction profile is obtained with the distribution given by

$$C(x,t) = \frac{C_0}{2} erfc(\frac{x}{2\sqrt{Dt}}) \quad \text{..... 4.9.3 [27]}$$

Where C_0 is the solid solubility limit of the dopant.

Diffusion for the proposed device was performed using 2 inch phosphorus solid source diffusion furnace using PD 900 source by saint gobain. This source is sued to get doping concentrations in the range of $1x10^{18}$ cm^{-3}. The brief procedure followed during the process is described below in Fig 4.5

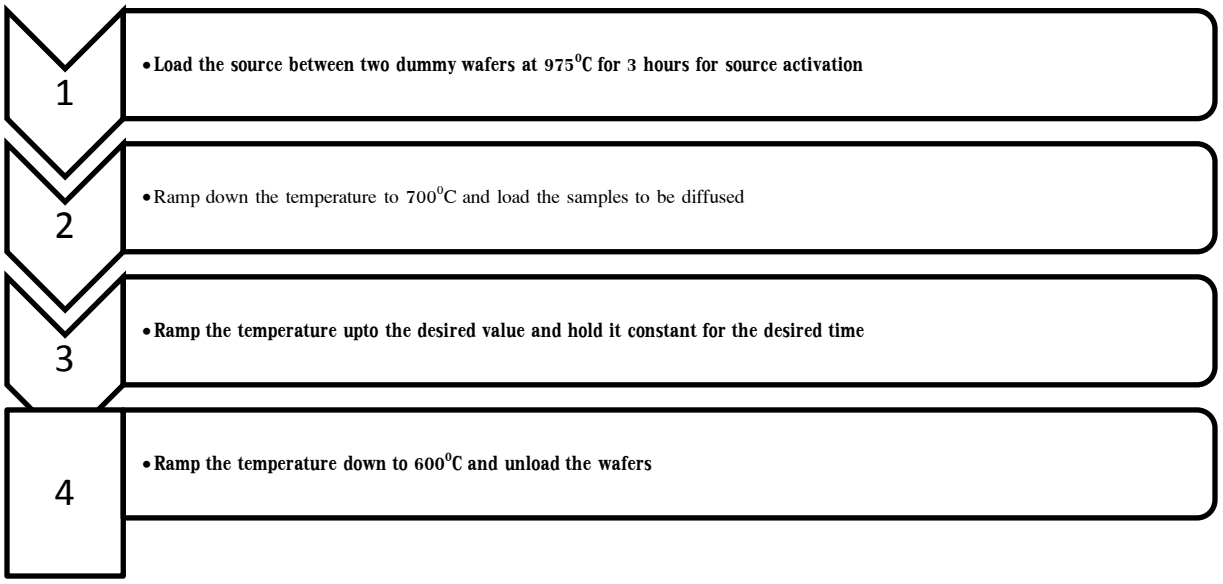


Figure 4.5: Process flow for Phosphorus Diffusion

4.10 Ion Implantation

Ion implantation is another way of introducing dopants into the substrate. This kind of implantation is used for more uniform and deeper doping. Plasma Immersion Ion Implantation (PIII) is a kind of Ion implantation that is basically used for non line of sight implantations [28]. The various terms and parameters used in the process is discussed below.

Plasma consists of charged ionized species. It consists of electrons, positive species and neural species. In the present system Phosphene gas (PH_3) and Diborane (B_2H_6) gases are used to create positively charged phosphorus and boron ions respectively. The wafer to be implanted is held at a negative potential for the dopant ions to be attracted and penetrate into its surface. The parameters that can affect the doping concentration and profile are

1. RF Power
2. Carrier Gas pressure
3. Distance between source and Substrate
4. Frequency
5. Pulse On time
6. Substrate bias
7. Implantation duration
8. Gas Flow

4.10.1 Carrier Gas pressure

It is very important parameter as it determines the ion dose. A very low pressure of around 1e-4 mbar the power of plasma is not enough to penetrate the surface and as the pressure increases the random collision increases thus increasing the amount of ions being able to implant into the substrate. Pressure of 1e-1 mbar is used throughout the process.

4.10.2 RF Power

The gases used in the implantation process get ionized in presence of RF power which is applied at a constant frequency of 13.6MHz. RF power of 1000W was used during the process of implantation.

4.10.3 Substrate Bias

The substrate bias is an important parameter in determining the junction depth of the implanted sample. The higher the substrate bias the more the acceleration of ions more deeper the implantation will be thus increasing the junction depth of the device. A constant substrate bias of -2KV was used throughout the process.

4.10.4 Implantation Duration

With increase in implantation duration the amount of ions that can be implanted increases thus increasing the concentration of the dopants in the sample. The ions used in the implantation have the property to etch out the silicon. As the sample gets saturated the etching of silicon becomes a predominant factor changing the device geometries at higher implantation durations [29]. Thus there must be optimization towards the implantation duration. Experiments with implantation durations from 15s to 60s were performed and the results obtained will be discussed in further chapters.

4.10.5 Pulse on Duration

When the substrate bias is applied the ion sheath expands and the ions are implanted into the substrate. This sheath expansion increases with increase in the substrate bias on time and can even interact with the source and etching also predominates at higher durations which alter the device geometry [29]. Hence there is a limitation on the amount of duration the bias on the substrate is turned on. The Pulse on duration was kept at 20us throughout the process.

4.10.6 Frequency of Substrate bias

The frequency of the substrate bias determines the number of times the sheath of ions expand thus implanting the ions into the substrate. The higher the frequency the higher is the sheath expansion thus increasing the dose of the implanted ions into the substrate. This is also accompanied by higher etching as more exposure to the ions is experienced. Frequencies of 1KHz and 5KHz was used during the process of experiment.

4.10.7 Distance between plasma and substrate

If the distance between the substrate and the plasma is less then when the sheath expands the sheath can touch the source of plasma which affects the ions penetrating into the substrate. Thus as the distance increases the sheath expands thus increasing the velocity, thus increasing the penetration depth. Thus more the distance between the plasma source and the substrate more is the penetration depth. A distance of 9cm was kept constant throughout the process.

4.10.8 Gas Flow

Gas flow was kept constant at 20sccm throughout the process.

4.11 Inductively Coupled Plasma Chemical Vapour Deposition (ICPCVD) for Oxide deposition

This method is used for Oxide deposition. The parameters used for the process depend on the desired thickness of the oxide. ICPCVD was used to deposit oxide as a protective layer for out diffusion during Rapid Thermal Processing (RTP) and as a isolation layer for metal pads.

The parameters used for different process is listed below.

Table 4.1: ICPCVD parameters for different oxide thickness

Parameter	Oxide for RTP	Oxide for Isolation
Forward Power(W)	40	40
Temperature(^{0}C)	31	35
Time(s)	10	140
SiH_4 Flow rate(SCCM)	16	16
Strike Pressure	25	30
Set Pressure	20	20
ICP power(W)	1000	1000
N_2O Flow rate(SCCM)	40	40
Thickness Of Oxide(nm)	14	105

4.12 Rapid Thermal Processing (RTP)

Once the samples are implanted because of high energy of ions used the crystal structure may be damaged. These dopants are now not in the crystal lattice points thus won't contribute to the electrical properties. When the samples are heated the implanted ions occupy the lattice points thus will contribute to the electrical activity of the semiconductor. This is called dopant activation. RTP was performed at 950^0C for 10s.

4.13 Metal Deposition using 4 Target E Beam Thermal evaporator

It is a process of metal deposition where in the target (wafer) is made as an anode and electron beam from the desired material is projected on to the anode(wafer) for a predefined time to get the desired thickness.

400nm of Aluminum was deposited in multiple steps. The process parameters used are

Chamber vacuum-$2.7x10^{-6}$ bar

Current-48mA

Temperature-71^0C

Voltage-4.35 KV

Table 4.2: Deposition time and thickness obtained in 4 Target E Beam Thermal evaporator

Time(minute)	Thickness(nm)	Rate(nm/min)
22	54	2.45
50	160	3.2
28	187	6.68

4.14 Metal deposition using Thermal evaporator (Al)

200nm of Aluminum was deposited by the process for backside contact. The process parameters are as below

Initial Vacuum-$5x10^{-2}$ mbar

High Vacuum during deposition-$5x10^{-6}$ mbar

Current-65 mA

Time-3 minutes

Thicnkess-200nm

4.15 Lift Off

Lift off is performed to obtain the metal contacts on the device after deposition is made on the entire wafer surface. Lithography was performed with the metal pad size of 50um x 50um required for electrical characterization using PPR. For effective lift off of the metal, the thickness of PPR should be at least 3 times the thickness of the metal deposited. An optimized recipe of 6000 RPM for 45s was used during spin Coating of PPR to obtain a thickness close t0 1.2um.

Lift off was done in acetone solution for 11 hours.

4.16 Annealing for alloying

Metal (Aluminum) once deposited on to silicon substrate has to be annealed to get a near Ohmic contact. The sample was annealed using Forming Gas (95% N_2, 5% H_2) for 30 minutes at 475^0C. N_2 gas at 2 LPM is used initially to create low pressure before loading the sample into the chamber.

4.17 Characterization

Once the implantation and diffusion is performed the characteristics have to be measured .A four probe system is a way of measuring the resistivity of sample. Secondary Ion Mass Spectrometry (SIMS) is used for measuring the amount of dopants induced into the sample. Profilometer is used to measure the crater depth obtained after the SIMS is done. IV characterization was done using Proxima fast IV measurement system within voltage limits of -20V to 100 V and with a current value between -20mA and 20mA. CV characterization was done using VEGA CV measurement system with voltage in the range of -1V to 5V.

Chapter 5

Results and Discussion

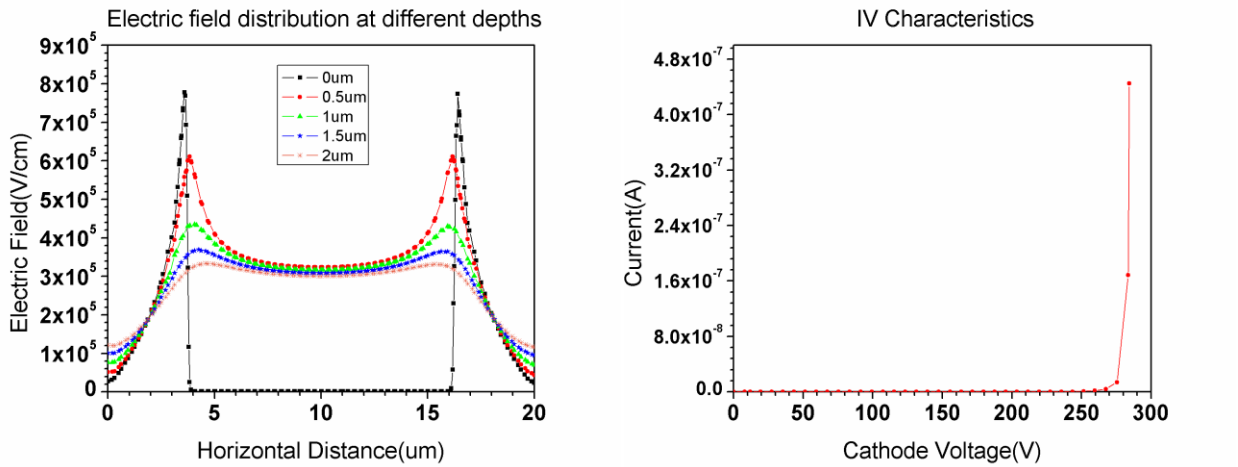
5.1 TCAD Simulation results

The various physics models used in TCAD simulations were earlier discussed in Chapter 3. Here a detailed look into results of the models used is discussed.

5.1.1 Electric Field distribution, IV characteristics and breakdown voltage for different physical models.

SRH Recombination Generation model with Doping and temperature dependence, auger Recombination Generation Model, band to band tunneling Model, mobility with dependence on Doping and electric field model were used in all the simulations for devices with and without guard rings with variations in the avalanche breakdown models.

5.1.1.1 Electric field distribution and IV Characteristics for Silicon Avalanche diode without guard rings



(a) (b)

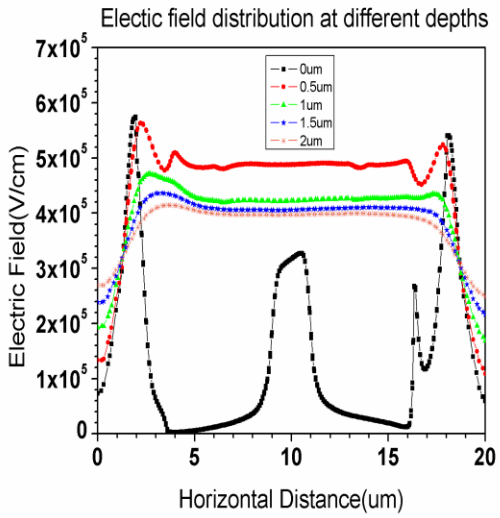
Figure 5.1: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode without Guard rings

From the above distribution it is seen that the corners of the doped region is high compared to the bulk regions

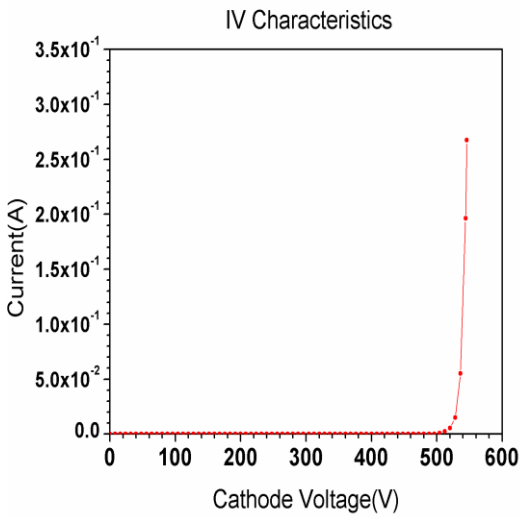
5.1.1.2 Electric field distribution and IV Characteristics for Silicon Avalanche diode with guard rings

Table 5.1: Models used for Avalanche breakdown simulation for devices with Guard rings

Model No	Models used
1	Avalanche Model-Okuto Crowell, Field Dependence of Avalanche Phenomenon-Parallel, SRH Recombination Electric Filed Dependence Model – None
2	Avalanche Model-Okuto Crowell, Field Dependence of Avalanche Phenomenon-Parallel, SRH Recombination Electric Filed Dependence Model-Schenk
3	Avalanche Model-Lackner, Field Dependence of Avalanche Phenomenon-Parallel, SRH Recombination Electric Filed Dependence Model-None
4	Avalanche Model-Lackner, Field Dependence of Avalanche Phenomenon-Gradient , SRH Recombination Electric Filed Dependence Model-None
5	Avalanche Model-Lackner, Field Dependence of Avalanche Phenomenon-Parallel, SRH Recombination Electric Filed Dependence Model-Schenk
6	Avalanche Model-Lackner, Field Dependence of Avalanche Phenomenon-Gradient , SRH Recombination Electric Filed Dependence Model-Schenk

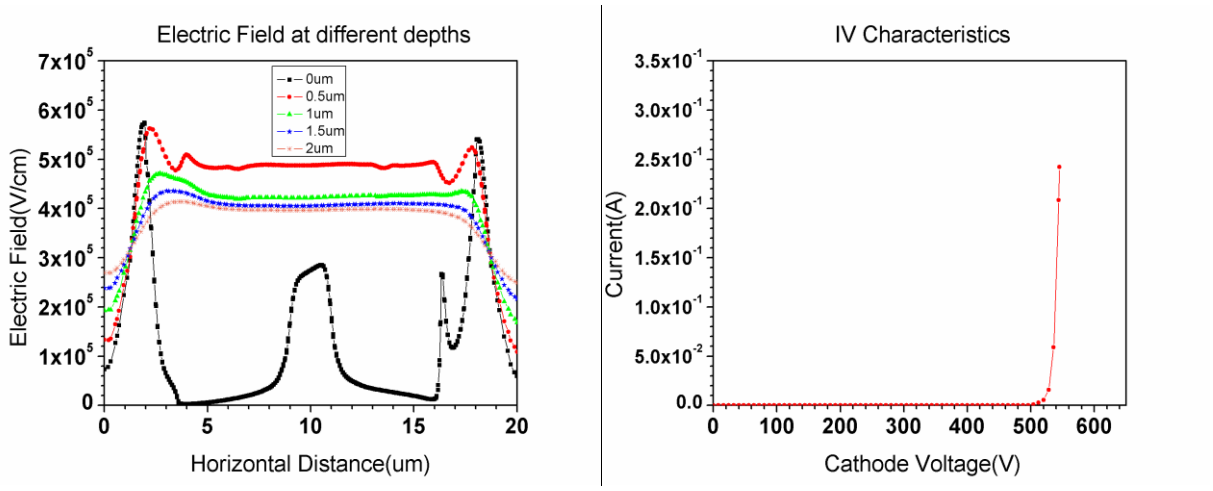


(a)



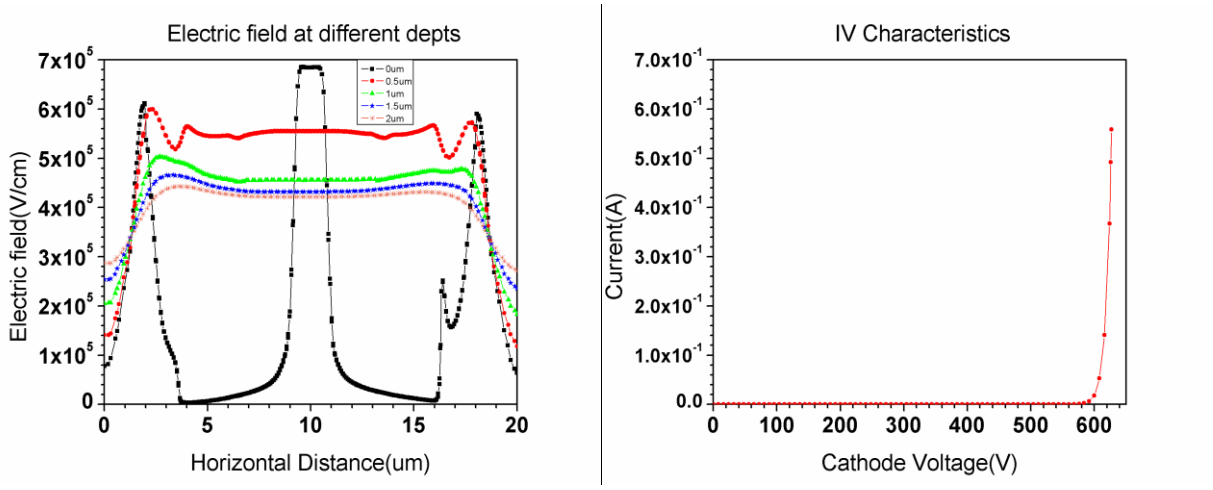
(b)

Figure 5.2: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 1 for Avalanche Breakdown Modeling



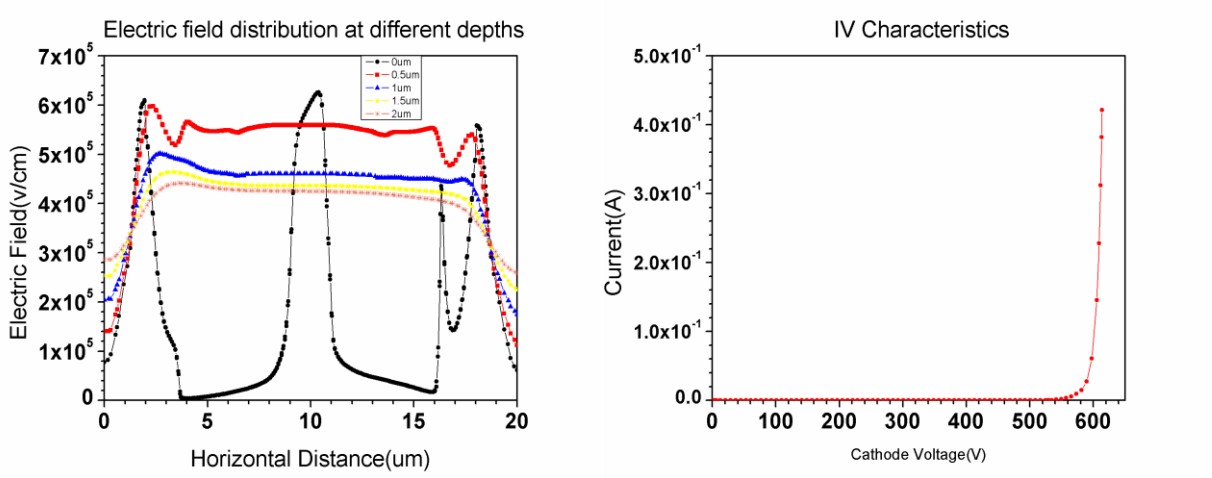
(a) (b)

Figure 5.3: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 2 for Avalanche Breakdown Modeling



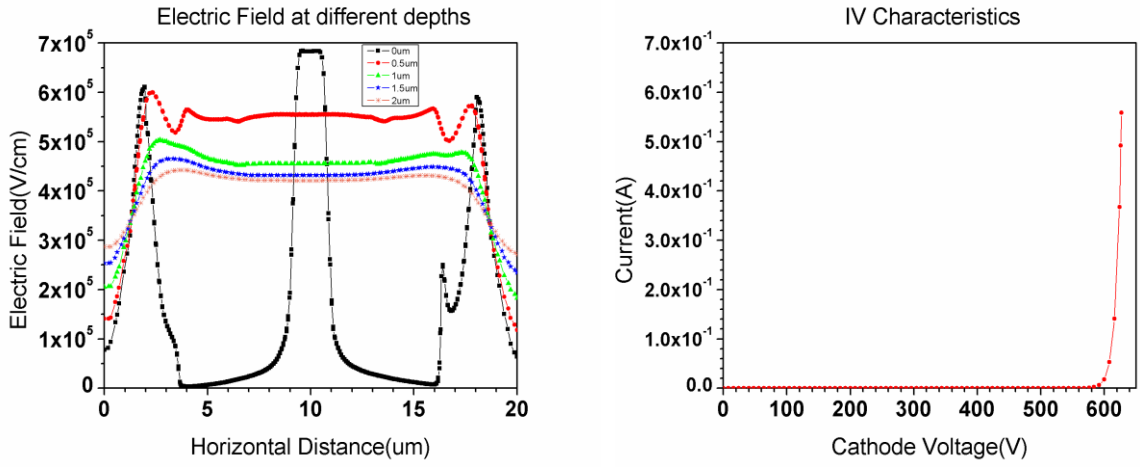
(a) (b)

Figure 5.4: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 3 for Avalanche Breakdown Modeling



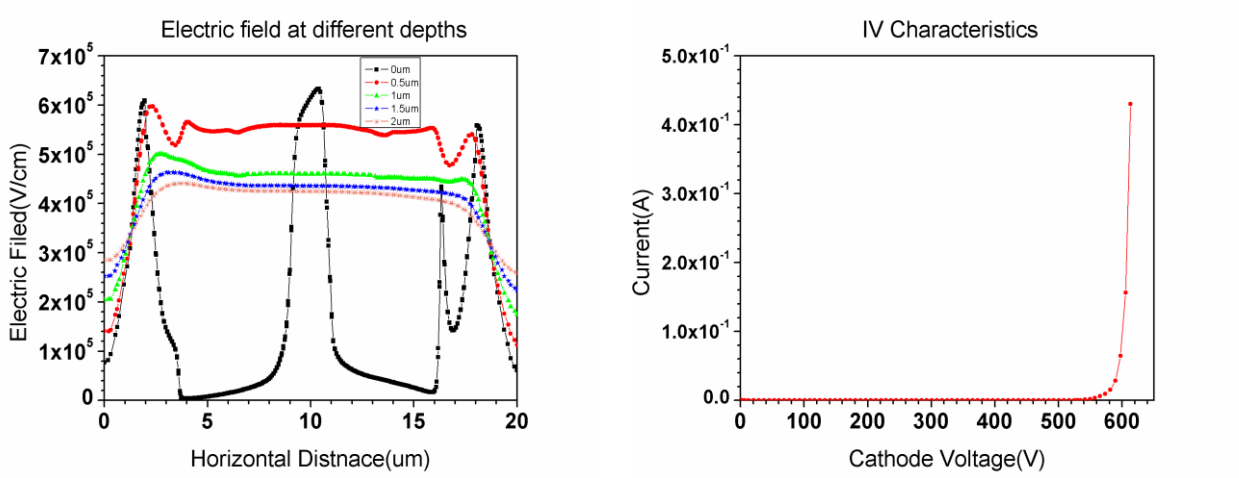
(a) (b)

Figure 5.5: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 4 for Avalanche Breakdown Modeling



(a) (b)

Figure 5.6: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 5 for Avalanche Breakdown Modeling



(a) (b)

Figure 5.7: (a) Electric Field distribution at different Depths (b) IV Characteristics of Silicon Avalanche Diode with Guard rings using Model 6 for Avalanche Breakdown Modeling

From the electric field distribution obtained for various models it is clear that with the use of guard rings uniform electric field is obtained throughout the active area of the device when compared to the devices without guard rings.

Table 5.2: Breakdown Voltages obtained for different models used

Model no	Breakdown Voltage(V)
1	505
2	505
3	630
4	540
5	630
6	540

The Lackner model when compared to Okuto model considers path length travelled by electron upon collision. This also takes into account the energy lost during the process. Thus more energy is needed for same current generation thus higher breakdown voltage is obtained. When gradient of the electric field is used the acceleration obtained due to the gradient increases the energy during the collisions thus decreasing the breakdown voltage.

5.2 Fabrication results

The fabrication process started with the optimization of the PIII parameters for Phosphorus implantation. A number of runs with the parameters indicated were done and the resistivities were measures at an approximate depth of 200nm. The active area of the device must be having a very high concentration, thus the parameters which gave higher concentration was used for the actual device fabrication.

Table 5.3: Parameters used for optimization of Phosphorus Implantation using PIII

Parameters	Sample 1	Sample 2	Sample 3	Sample 4
Substrate Bias(KV)	-2	-2	-2	-2
Frequency(KHz)	5	1	5	5
Pulse on Duration(us)	20	20	20	20
Distance(cm)	9	9	9	9
Gas pressure(mbar)	$1x10^{-1}$	$1x10^{-1}$	$1x10^{-1}$	$1x10^{-1}$
RF Power(W)	1000	1000	1000	1000
Carrier gas flow(sccm)	20	20	20	20
Implantation Duration(s)	25	15	60	90
Resistivity (Ohm-cm)	$3.22x10^{-2}$	$5.55x10^{-2}$	$1.5x10^{-2}$	$3.23x10^{-2}$

All the above implantations were done on P-Type <100> Double side polished 4-7 Ohm cm wafers. From the above it is observed that sample -3 would give the lowest resistivity, thus these parameters were used for further device process.

In SIMS measurement count of the desired species to the implantation time is obtained. The conversion from the implantation time to implantation depth has to be made by measuring the depth of implantation and converting the depth to etch rate of the sample and calculating the distance corresponding the time of implant. The counts to concentration conversion is to be made using standard conversion parameters and the conversion factor was found to be

1 count= $2.8986x10^{17}$ cm^{-3} for Boron in silicon and 1 count= $2.9197x10^{17}$ cm^{-3} for Phosphorus in silicon.

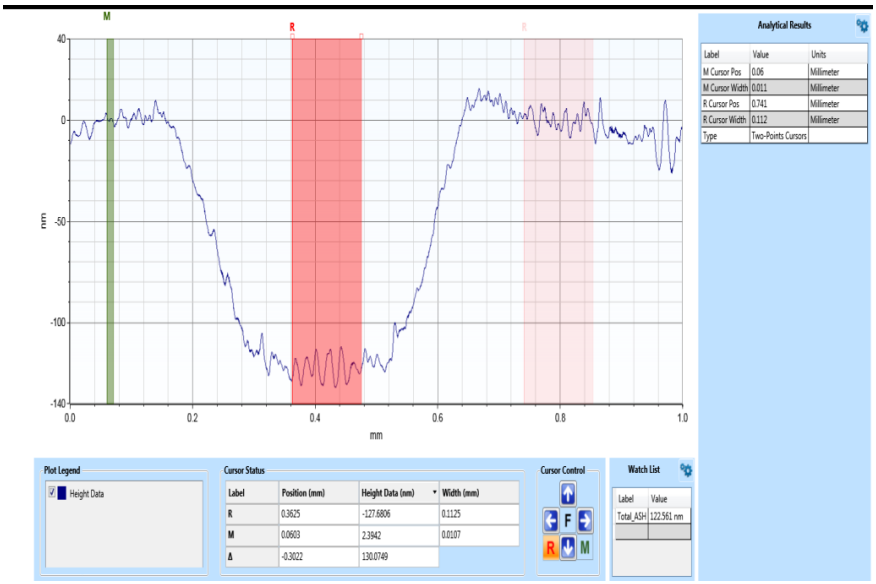


Figure 5.8: Profilometer depth profile for un annealed Phosphorus Implanted sample

The profilometer measurement for unannealed sample indicating average depth 120nm, with the sputter time of 650s.

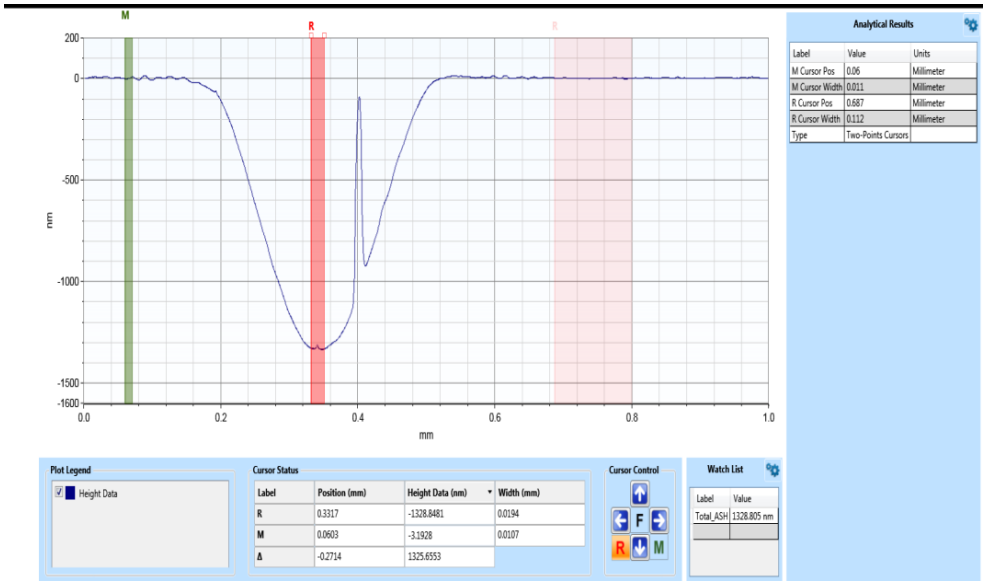


Figure 5.9: Profilometer depth profile for Phosphorus Implanted sample and annealed at 650^0C for 30s

The profilometer measurement for annealed sample indicating average depth 1300nm , with the sputter time of 2180s.

The doping profile after implantation and annealing is as shown in Fig 5.10

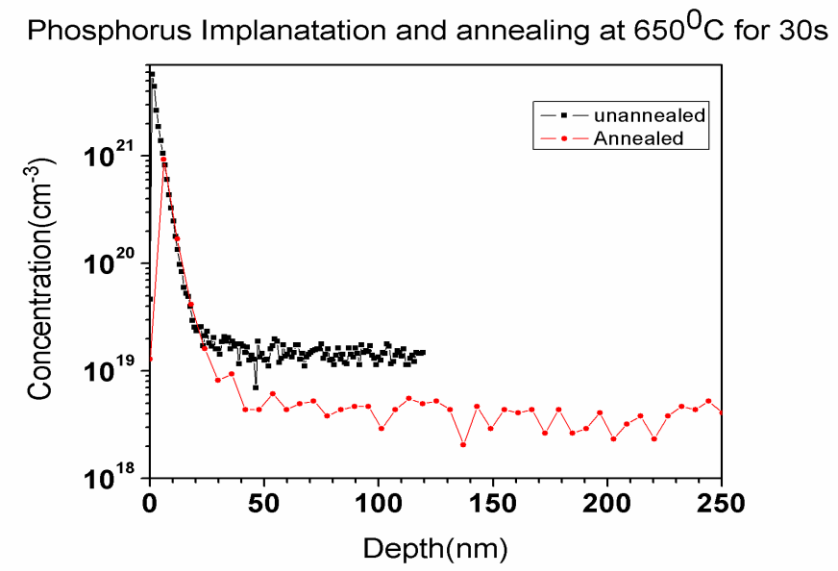


Figure 5.10: SIMS profile for 650^{0}C annealing and un annealed phosphorus sample

From the figure it is observed that the in the annealed sample has lower concentration but the profile of both the samples remains almost same. So higher temperature annealing is needed for broader distribution and more penetration of atoms into the silicon sample.

Implantation was also performed on 1-5 Ohm cm wafers and annealed at 950^{0}C for 10s. The results obtained are given below.

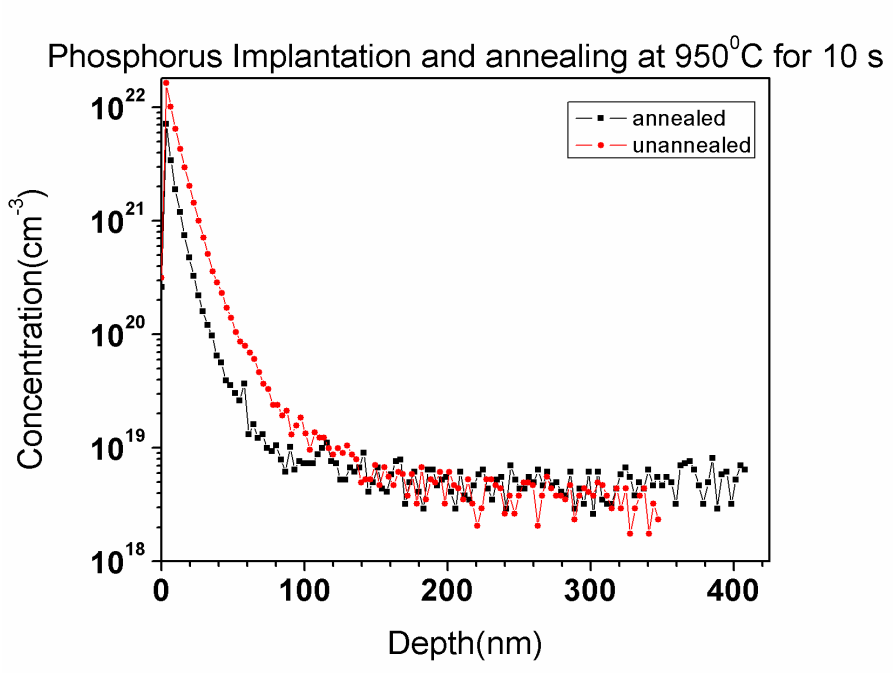


Figure 5.11: SIMS profile for 950^{0}C annealing and un annealed phosphorus sample

The profile distribution of dopants is much steeper in case of annealed sample which was not expected. This can be attributed to out diffusion of dopants. This can be avoided by depositing a small thickness of oxide.

The diffusion of Phosphorus was performed using source PD 900 at temperature 850^0C and 900^0C for 15 minutes. The resistivity measurements yielded $8.9x10^{-2}$ ohm cm and $1.3x10^{-2}$ ohm cm respectively at 850^0C and 900^0C respectively. The resistivity measurements might not be exact as we get a more distributed profile in diffusion process. SIMS profiling was done on both the samples. The detection capability of SIMS in SAIF IIT Bombay is limited to around 10^{18} cm^{-3}. Hence the detection of Phosphorus in sample processed at 850^0C was not successful. The sample at 900^0C showed the presence of phosphorus with concentration of around 10^{18} cm^{-3} which meets the desired required value for the proposed device, though the exact profile of the diffused sample was not obtained.

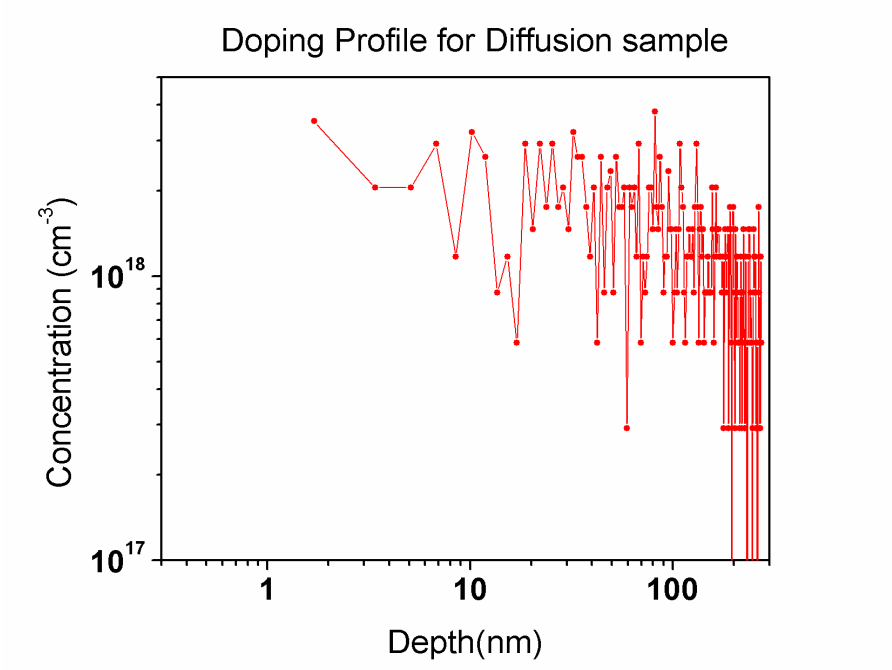


Figure 5.12: SIMS Profile for Phosphorus Diffusion

Boron Implantation was done with similar parameters used for Phosphorus implantation with implantation duration of 30s and 60s respectively. The resistivity measurements on both the samples yielded $5.187x10^{-3}$ Ohm cm and $4.96x10^{-3}$ Ohm cm for 30s and 60s respectively. Thus the 60s implantation would be giving the desired higher concentration.

The sample was annealed at 950^0C for 10 seconds in nitrogen ambient. The profile is indicated in Fig 5.13 .

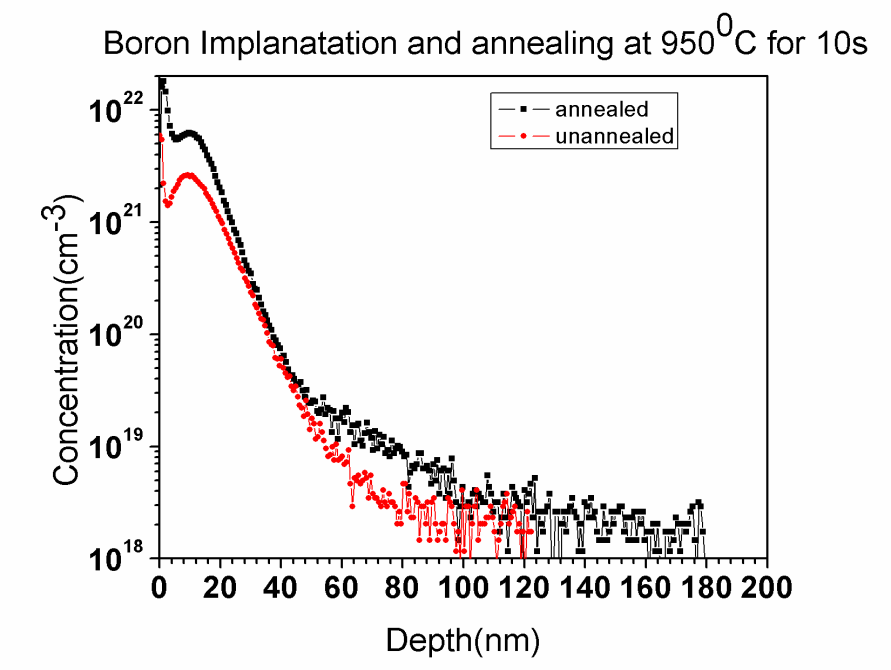


Figure 5.13: SIMS profile for 950^{0}C annealing and un annealed boron sample

The above SIMS profile indicates the wider distribution of dopants after annealing

5.2.1 Resistivity to doping concentration conversions

Resistivity of the implanted samples were measured using four probe measurement system. The minimum depth that could be specified for measurement in the system was 10nm. The concentration of the could be related to the resistivity with the relation

$$\rho = \frac{1}{(nu_n\, e + pu_p\, e)} \quad \text{.....5.2.1.1 [27]}$$

Where ρ is the resistivity, n and p represents the concentration of electrons and holes respectively, u_n and u_p represents the mobility of electrons and holes respectively and e is the electrical charge. The conversion from resistivity to concentration generally gives the concentration of majority carrier in the doped sample.

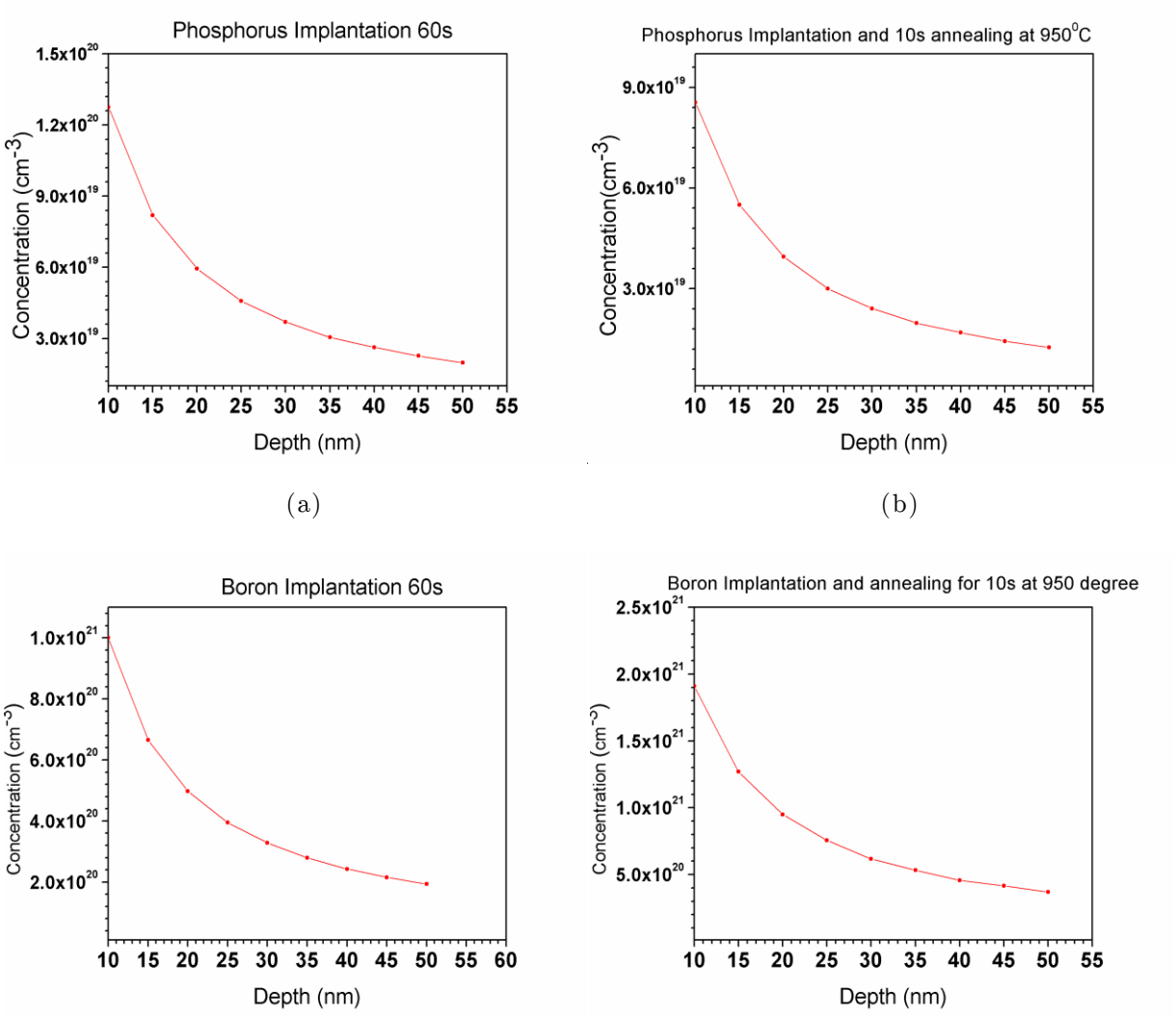
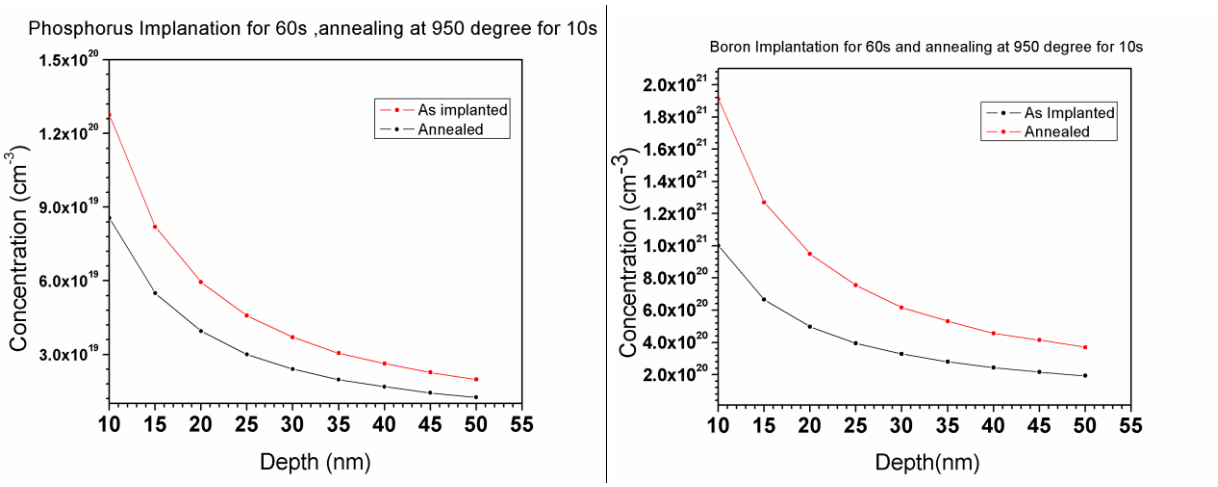


Figure 5.14: Resistivity to Doping concentration conversion a) As implanted phosphorus b) As annealed phosphorus c) As implanted boron d) As annealed boron



(a) (b)

Figure 5.15: Resistivity to Doping concentration conversion a) Phosphorus implanted sample b) Boron implanted sample

From Fig 5.14 and 5.15 we get an approximate profile for the implanted samples, which can be used for calculations in absence of Sophisticated analytical instruments.

5.2.2 FESEM Images of the Fabricated Devices

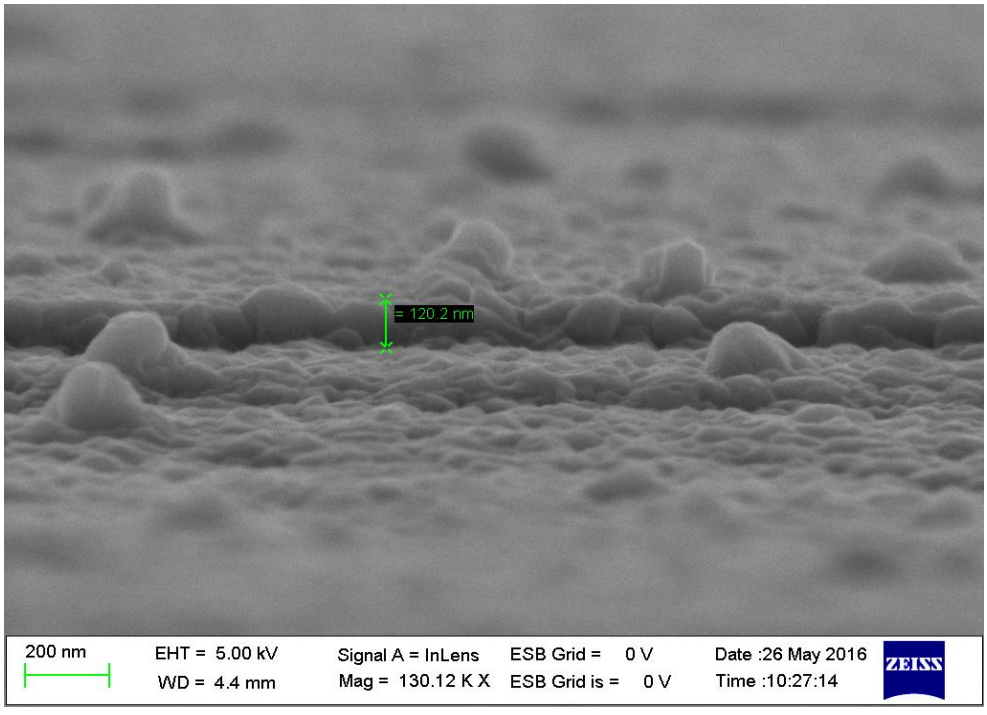


Figure 5.16: Cross-sectional FE-SEM image indicating etch depth of 120nm of at places where actual devices were present

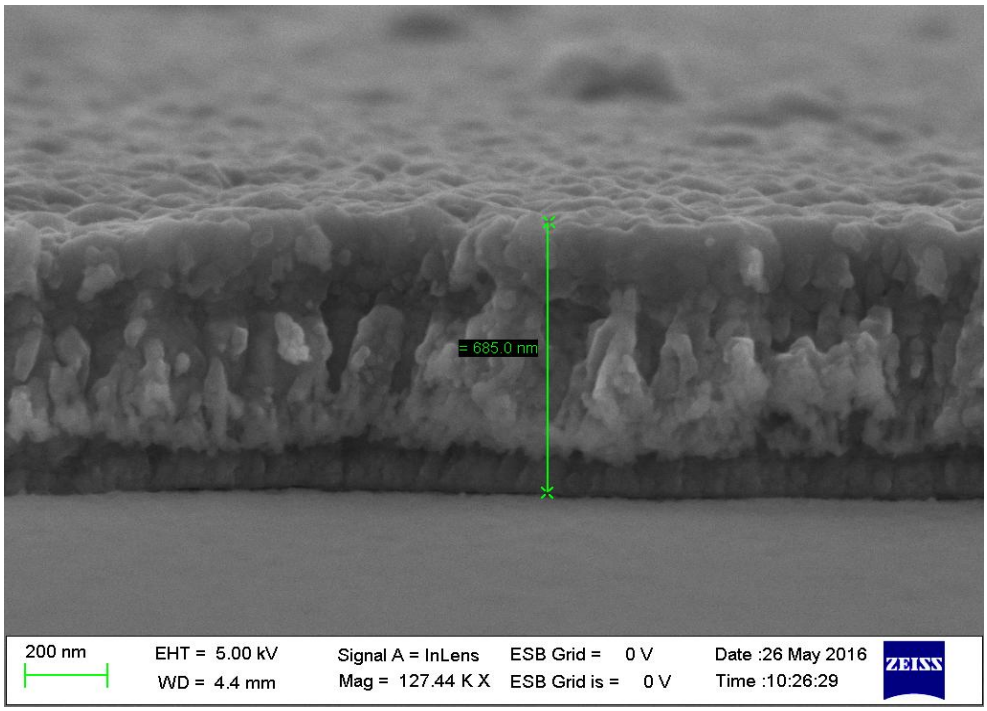


Figure 5.17: Image Indicating presence of two layers Oxide and Aluminum with total thickness of 685nm indicating thickness of Aluminum close to 460nm

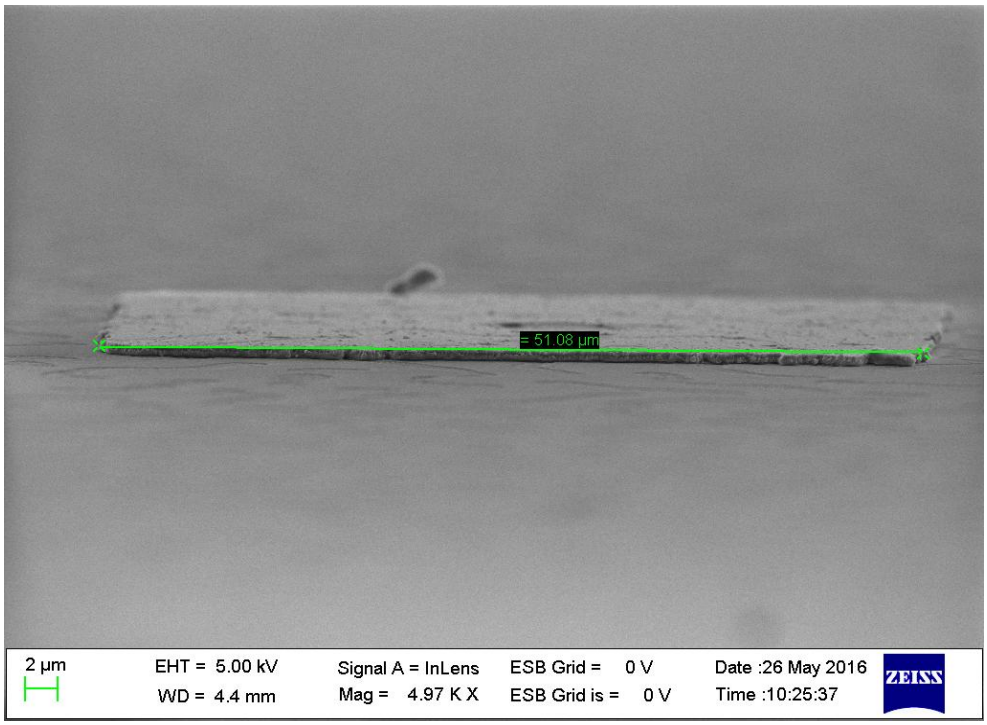


Figure 5.18: Cross section of Metal Pads used for electrical Characterization

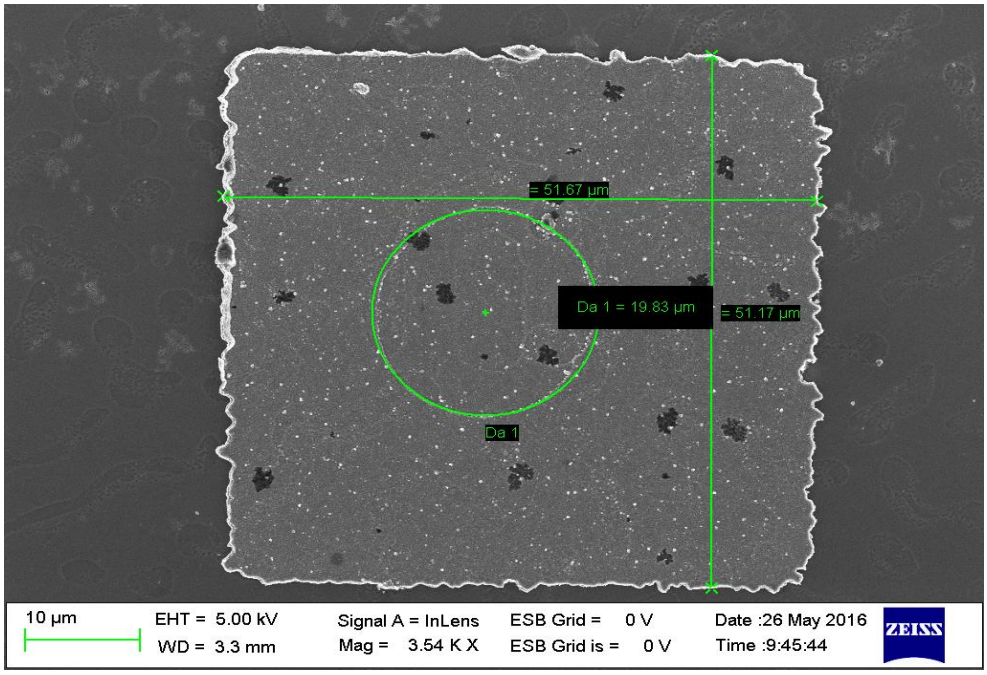


Figure 5.19: Top View Of Metal Pads Used for Electrical Characterization

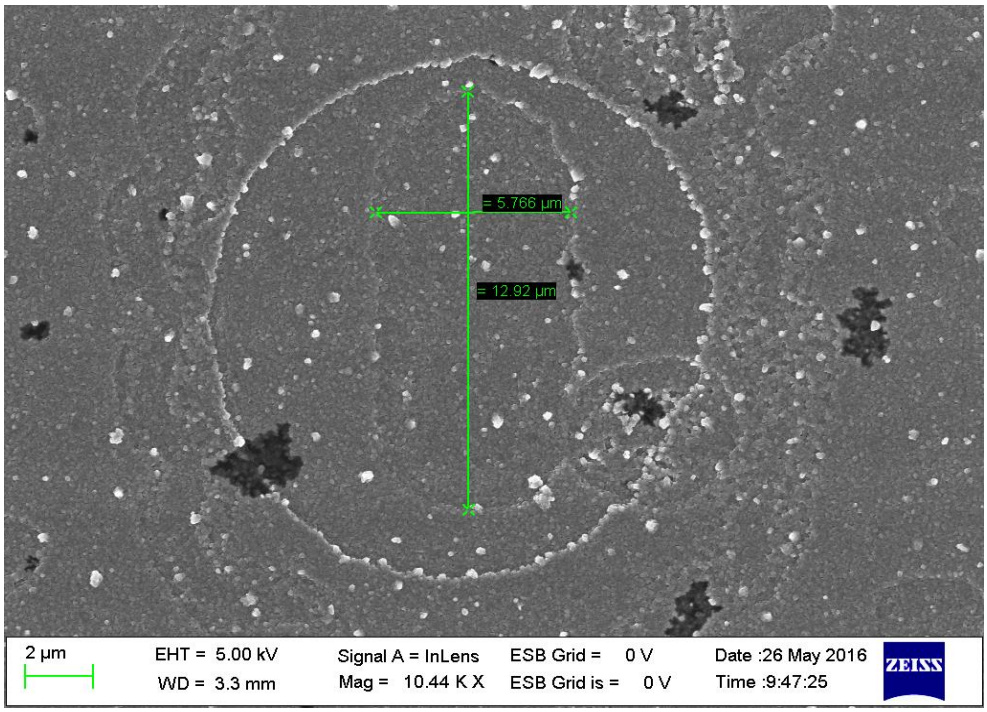


Figure 5.20: Implanted Area Indicated by a visible mark on the wafer

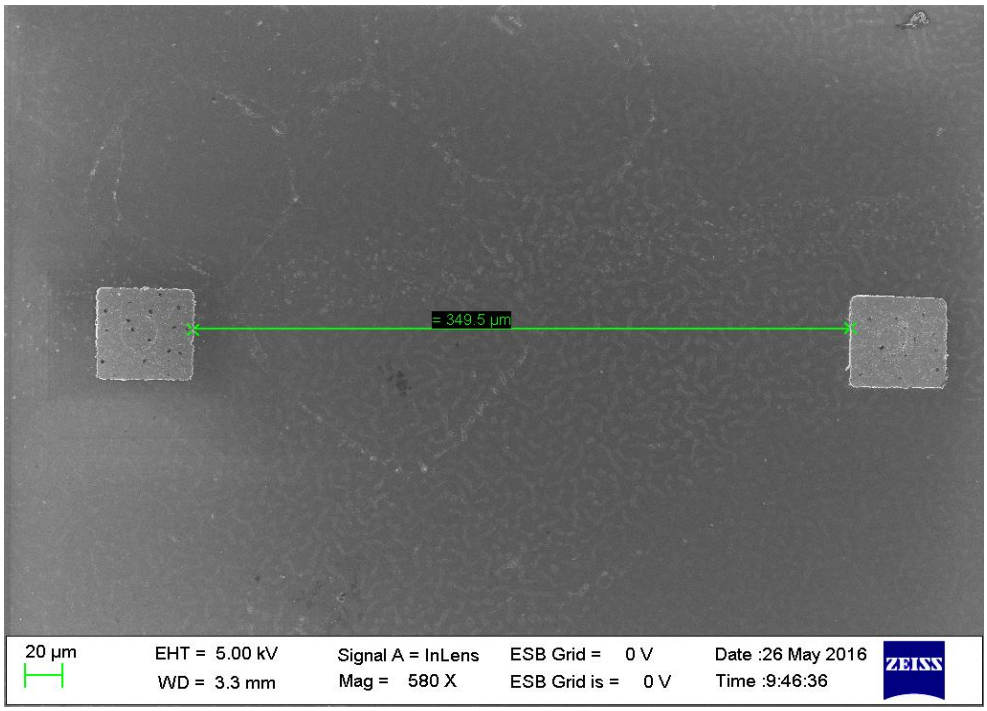


Figure 5.21: Devices Separated by 350um in the horizontal direction

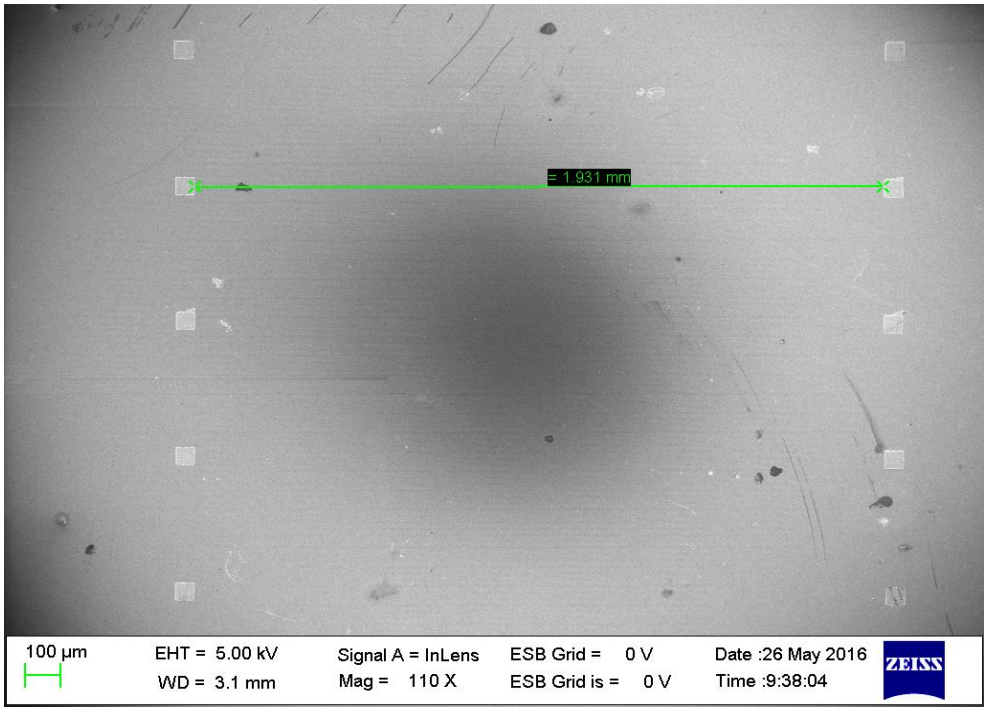


Figure 5.22: Array Of devices in different columns separated by a distance of close to 2mm

5.2.3 Electrical Characterization of the fabricated devices

With the various steps mentioned in the previous chapter Avalanche diode with and without guard rings were fabricated. The IV and CV Characteristics obtained are included below.

Devices without Guard rings

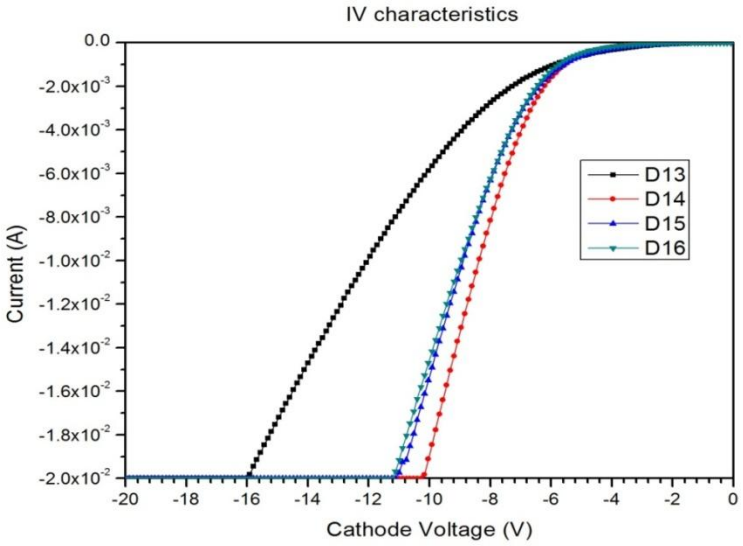


Figure 5.23: Forward Bias Characteristics of device without guard rings

Table 5.4: Diode Parameters from forward bias characteristics of device without guard rings

Device no	Series Resistance(Ohm)	Ideality factor	Cut-in Voltage (V)
D13	681	8.41	5.5
D14	414	4.76	5.7
D15	460	5.49	5.5
D16	472	5.56	5.9

The junction was created using ion implantation in plasma environment. This creates trap sites which can be attributed to the high ideality factor of the devices.

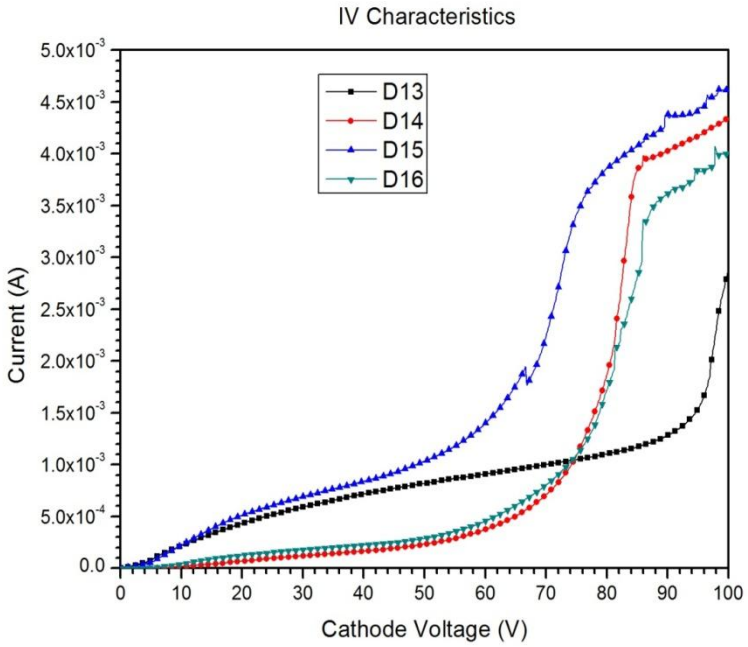


Figure 5.24: Reverse Bias Characteristics of device without guard rings

Table 5.5: Diode Parameters from reverse bias characteristics of device without guard rings

Device no	Breakdown Voltage(V)	Current at breakdown voltage I(mA)	Current I_0(A)	$I_{AV,}$ Current at voltage $5nV_T$	Avalanche Gain=I/I_{AV}	Factor n
D13	90	1.2839	$4.07652x10^{-7}$	$9.907x10^{-6}$	129.59	8.7397
D14	76.24	1.2500	$3.5894x10^{-11}$	$5.823\ x10^{-10}$	$2.146x10^{6}$	$2.9x10^{-4}$
D15	59.92	1.3955	$3.05618x10^{-8}$	$3\ x10^{-6}$	465.1666	1.0792
D16	72.04	0.9077	$2.80944x10^{-8}$	$5.527x10^{-7}$	$1.642x10^{6}$	$3.6x10^{-7}$

Some of the devices had higher leakage current can also be attributed to the trap states present in devices due to effect of plasma. The breakdown voltage obtained is much less than what is obtained in simulations. In simulations a controlled distribution profile can be obtained for dopants, which could not be exactly reproduced during fabrication. A steep profile was obtained which might be attributed for lower breakdown voltage that is obtained for the devices.

Devices with Guard rings

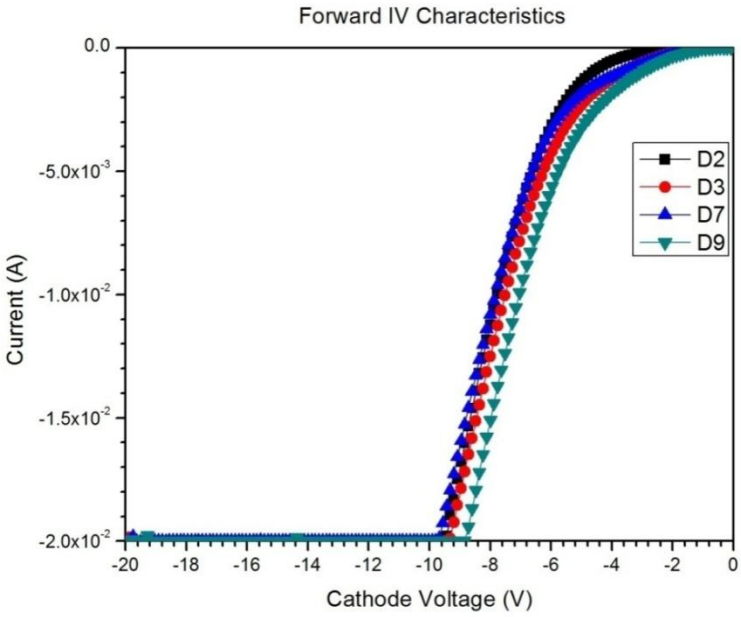


Figure 5.25: Forward Bias Characteristics of device with guard rings (set-1)

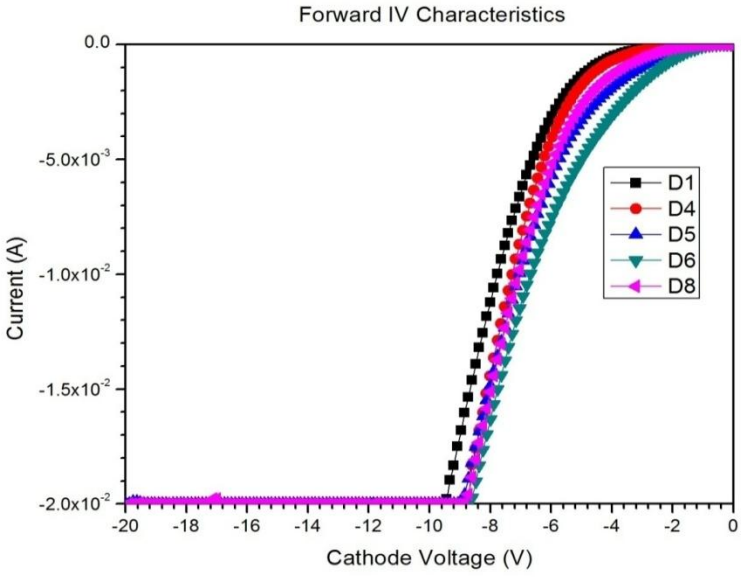


Figure 5.26: Forward Bias Characteristics of device with guard rings (set-2)

Since the intended devices are the ones with the guard rings more devices were characterized and the device characteristics obtained are indicated below.

Table 5.6: Diode Parameters from forward bias characteristics of device with guard rings (set-1 & set-2)

Device	Current Io(A)	Series Resistance(Ohm)	Ideality Factor	Cut-in Voltage(V)
D1	$3.234x10^{-10}$	413	2.9154	4.6
D2	$1.3363x10^{-13}$	363	1.6898	2.8
D3	$5.2769x10^{-12}$	412	2.319	3.9
D4	$5x10^{-11}$	370.5	2.9528	4.5
D5	$3.855x10^{-10}$	388	2.5742	3.7
D6	$1.2442x10^{-10}$	376	3.7	2.5
D7	$6.4x10^{-12}$	440	1.79	5.2
D8	$6.34x10^{-10}$	364.5	3.7	4.1
D9	$3.597x10^{-11}$	397	2.08	3.8

From the parameters in Tables 5.4, 5.5 and 5.6 it is evident that the leakage current is predominantly lesser in device with guard rings and show better ideality factor. The presence of guard rings and uniform electric field it introduces in the device can be attributed to these characteristics of the devices.

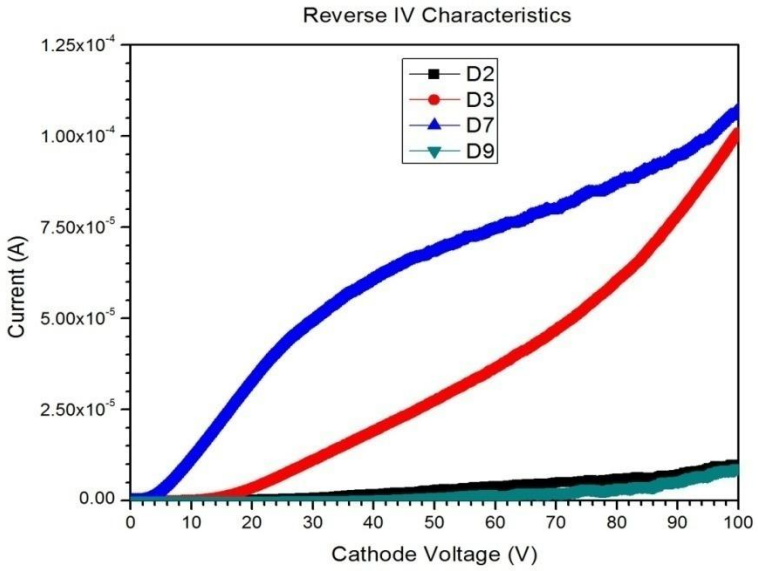


Figure 5.27: Reverse Bias Characteristics of device with guard rings (set-1)

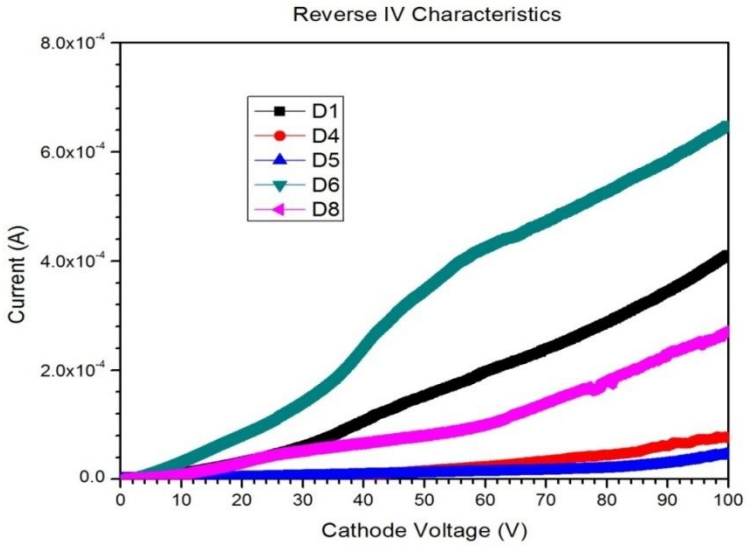


Figure 5.28: Reverse Bias Characteristics of device with guard rings (set-2)

From the graphs and the characteristics obtained, the breakdown phenomenon is not being seen. The leakage current obtained also is less when compared to the devices without guard rings. From the gain characteristics obtained in the devices without guard rings it was evident that lesser the leakage current higher would be the avalanche gain. Thus devices with guard rings would naturally be having higher gain around the breakdown voltage if used when compared with those without them. Thus the use of devices with guard rings can be in general used in applications that require very high sensitivity and because of the increased breakdown voltage that is being shown in the characteristics it can also be used in applications that require higher stability.

Few devices with guard rings were obtained with breakdown characteristics were obtained for voltages less than 100V, but the breakdown voltages obtained were higher than those of devices without guard rings. The characteristics of those devices are discussed in the next section

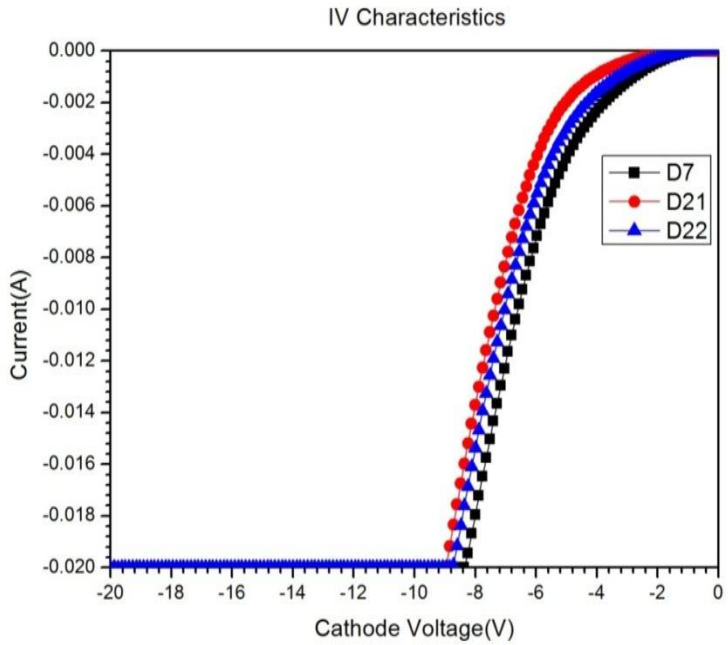


Figure 5.29: Forward Bias Characteristics of device with guard rings (set-3)

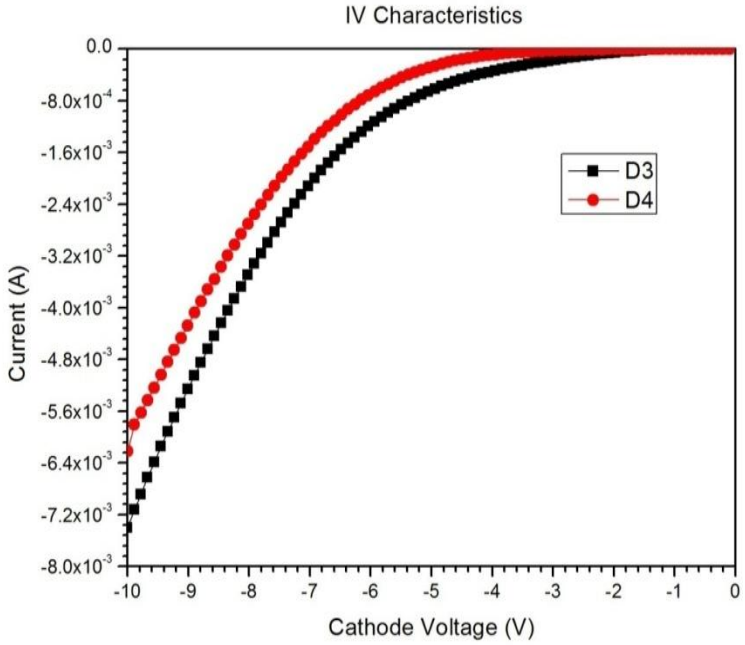


Figure 5.30: Forward Bias Characteristics of device with guard rings (set-4)

Table 5.7: Diode Parameters from forward bias characteristics of device with guard rings (set-3 & set-4)

Device no	Series Resistance(Ohm)	Ideality factor	Cut-in Voltage (V)
D3	1108.1	3.46	5.1
D4	1382.52	3.59	5.5
D7	363	1.695	2.8
D21	394	1.68669	4
D22	386	2.74	3.8

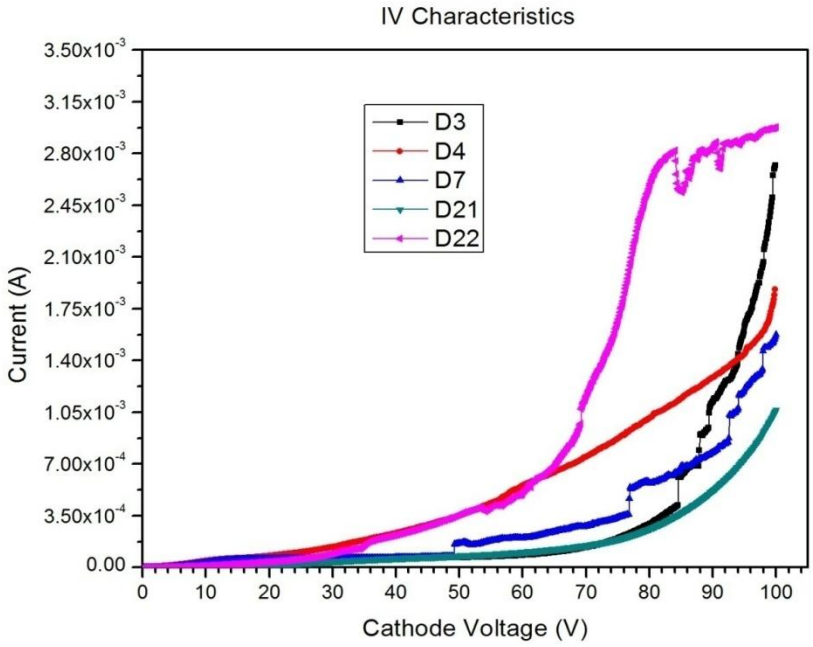


Figure 5.31: Reverse Bias Characteristics of device with guard rings (set-3 & Set 4)

Table 5.8: Diode Parameters from reverse bias characteristics of device with guard rings (set-3 & set-4)

Device no	Breakdown Voltage(V)	Current at breakdown voltage I(mA)	Current I_0(A)	I_{AV}, Current at voltage $5nV_T$	Avalanche Gain=I/I_{AV}	Factor n
D3	87.02	0.6959	$1.1682x10^{-10}$	$5.507x10^{-8}$	$12.63x10^{5}$	0.0633
D4	96	1.4904	$4.9913x10^{-10}$	$8.640x10^{-7}$	1725	0.7590
D7	81.88	0.5939	$1.5259x10^{-11}$	$4.073x10^{-10}$	$1.458x10^{6}$	$4.6x10^{-4}$
D21	79.96	0.2603	$2.4087x10^{-11}$	$1.031x10^{-10}$	$2.524x10^{6}$	$2.6x10^{-4}$
D22	66.04	0.7521	$3.178x10^{-12}$	$4.886x10^{-9}$	$1.539x10^{5}$	0.0036

From the CV characteristics in Fig 5.32 it is clear that the capacitance is almost constant for voltages in the reverse bias condition which are positive voltage ranges in the present situation. Thus the obtained CV characteristics for the diode is in lines with the ideal characteristics of the diode. The junction capacitance obtained is close to 9.5Pf in most of the devices.

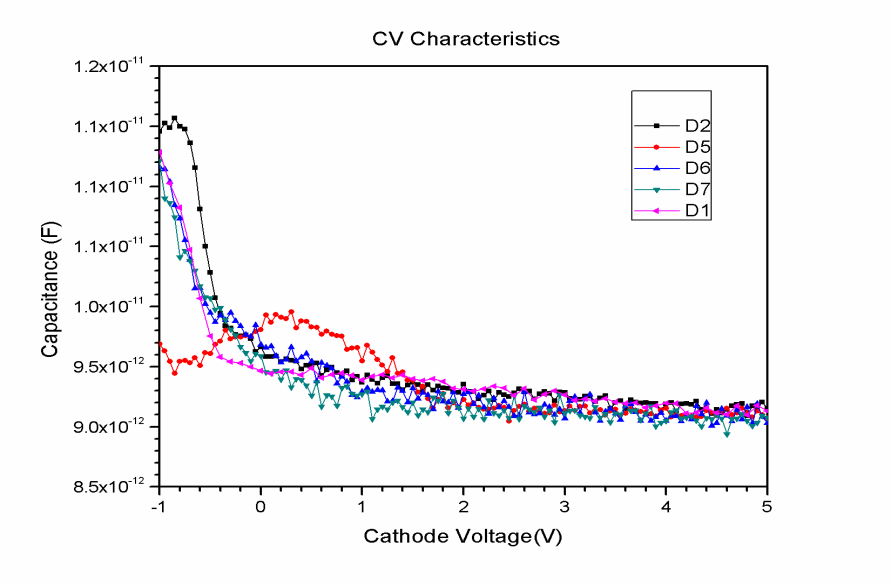


Figure 5.32: CV Characteristics for Devices with and without guard rings

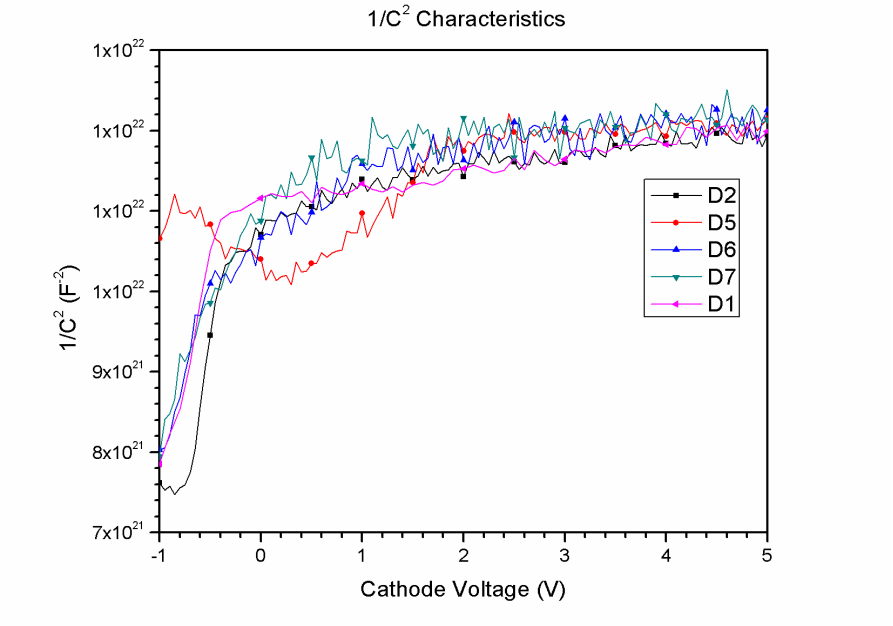


Figure 5.33: $1/C^2$ Characteristics for Devices with and without guard rings

The $1/C^2$ characteristics which exhibit a non uniform symmetry indicates non uniform doping around the junctions which is as expected from the SIMS profile obtained for doping.

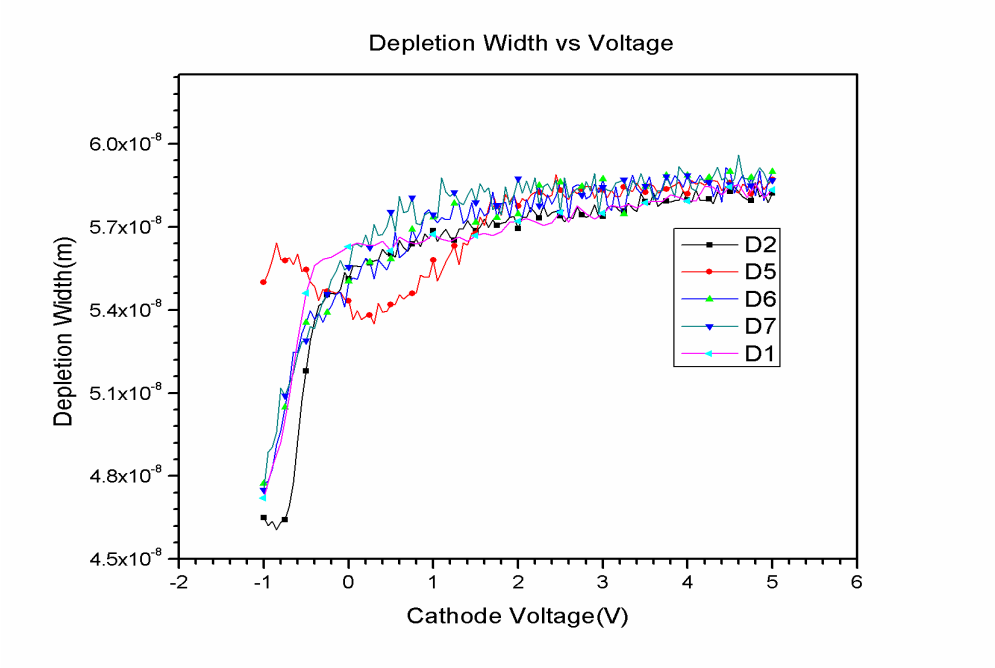


Figure 5.34: Variation of depletion width with cathode voltage

A metal pad of 50x50 um was used for probing the devices. The devices fabricated have a spherical symmetry so the area of metal pads was equated to that of a circle to get its radius. The effective area was calculated using the radius obtained and the Depletion width corresponding to different voltages were calculated using the capacitance obtained for the applied voltages using the model of a parallel plate capacitor the results obtained are as indicated in Fig 5.34

5.3 Bombardment Gain

The bombardment gain depends on the incident electron energy on the Silicon. The electron looses energy as it passes through the Aluminum contact. The maximum thickness for given acceleration of electron that can be used before the electron energy drops to zero depends on the stopping power of the Aluminum layer for given incident energy. The electron energy loss for different thickness is obtained by multiplication of thickness with stopping powers. The electron energy at the surface of Silicon is difference between the incident energy and the energy lost in the aluminum layer.

Table 5.9: Maximum thickness of aluminum that can be used for given electron acceleration

Incident Electron Energy(KeV)	Maximum Aluminum Thickness(A^0)
1	416
2	1219.5
4	4008
6	8152.17
8	13559.3
10	20202

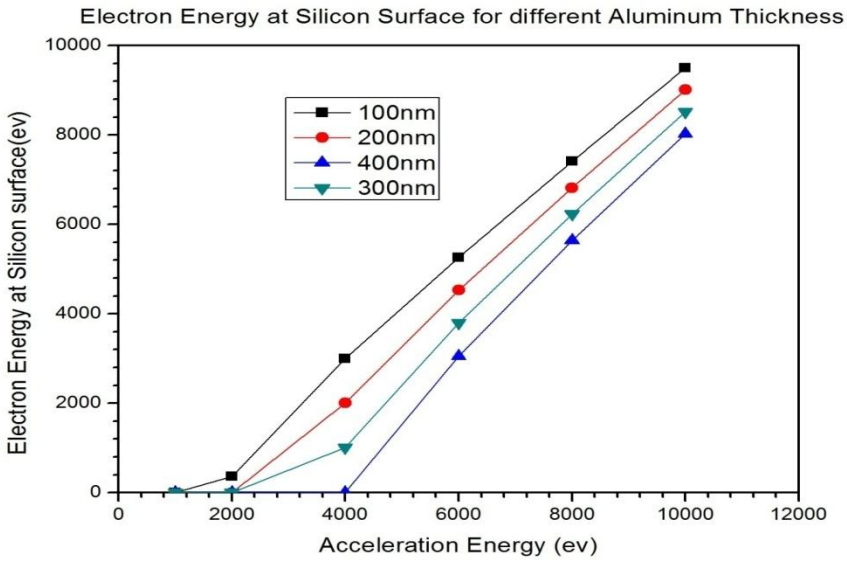


Figure 5.35: Electron Energy at surface for different aluminum thickness

The Bombardment Gain is given by the electron energy at the Silicon surface by 3.6ev (Energy needed to create an electron hole pair). The Comparison of gain for different Aluminum Thickness is given below

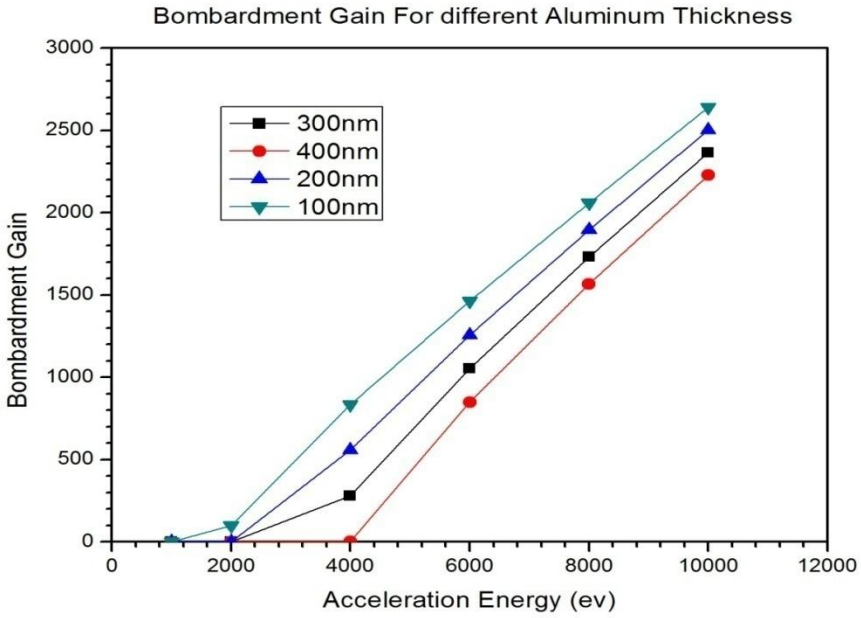


Figure 5.36: Variation of Bombardment gain with acceleration voltage for different aluminum thickness

5.4 Gain of the Hybrid Photo detector

From the characteristics described in the previous sections the bombardment gain can vary in the range close to 2500 and the avalanche gain is obtained in the order of 10^6 in some devices. The overall gain being the product of bombardment and the avalanche gain we can expect the gain of the proposed Hybrid Photo Detector in the order 2.5×10^9.

Chapter 6

Conclusion and Future work

6.1 Conclusion

In this work the Si Avalanche Diodes with Guard rings were successfully fabricated using a CMOS compatible process as a substrate for electron Bombardment and as a avalanche electron multiplier in hybrid-photo diode applications. It is also shown from the simulated results that the uniform electric field is obtained by the use of guard rings which in effect avoids the premature breakdown of the devices which was verified from the reverse characteristics of the fabricated devices where the devices without guard rings showed early signs of breakdown when compared to the devices with guard rings. This shows an improved stability of the system involving avalanche diode with guard rings. From the IV characteristics it is also seen that the devices with guard rings show closer behavior to the ideal diodes, which could be verified by the calculations of ideality factor and the leakage current. The leakage current is devices with guard rings is less because of the uniform electric field throughout the active region of the device, as the higher electric at some parts of device could trigger unwanted current in Off state, thus the use of guard rings in reducing the leakage current is also presented in this work.

It is also seen from the results obtained that the avalanche gain was higher for devices with low leakage current. Since from the characteristics obtained it shown that devices with guard rings contribute less leakage current we can conclude that the devices with guard rings also improve the avalanche gain of the device. The gain characteristics also show high bombardment gain with increase in the acceleration of the electrons. We can conclude that the combination of high acceleration of electrons from the photocathode leads to high bombardment gain onto the silicon substrate with further enhancement in the gain achieved by using avalanche diode with guard rings to get gain in the range of 2.5×10^8 leading to the use of the proposed hybrid photo detector in highly sensitive applications.

6.2 Future work

Silicon Avalanche Diode as a multiplier was fabricated as a part of this work. Theoretical calculations with respect to the bombardment gain which were also done in this work need to be verified by physically bombarding highly accelerated electrons onto the silicon substrate. The first point of impact of the photons to be detected by the hybrid photo detector is the III-V semiconductor photocathode. The photocathode material which depends on the wavelength of

the target wavelength of detection has to be selected and has to be tested for its quantum efficiency as this affects the overall sensitivity of the detector and ways to increase the existing quantum efficiency has to be looked into. The theoretical and the experimental results obtained in the previous sections are in conditions of high vacuum. The detector is stable and sensitive as proposed in the previous sections only under the high vacuum condition. Thus the photocathode and the silicon avalanche diode has to be housed in a chamber with high vacuum capabilities with the outer casing being magnetically and electrically inactive so that no extraneous photons enter into the system other than from the actual entrance of the system and also no change in the electron trajectory as it travels from the photocathode onto the silicon avalanche diode.

With all the above conditions satisfied there is necessary to measure the number of charges generated by impact of photon onto the detector and the response time of the sensor is to be calibrated. The design of highly sensitive read out circuit to be integrated onto the detector also needs done as a part of the entire design flow of the hybrid photo detector.

Reference

[1] Photomultiplier Tubes Basics & Application, HAMAMATSU, THIRD EDITION (Edition 3a), August 2007

[2] G.A.Johansen, C.B.Johnson, "Operational Characteristics of Silicon Diode Photomultiplier Tube", *Nuclear Instruments and Methods in Physics Research*, A326, pp.295-298, 1993.

[3] High Speed Compact Detector, HAMAMATSU, http://www.hamamatsu.com/resources/pdf/etd/R10467U-40_R11322U-40_TPMH1337E01.pdf

[4] Ehsan Kamrani, Fredric Lesage, Mohamad Sawan, "Premature Edge Breakdown Prevention Techniques in CMOS APD Fabrication", *New Circuits and Systems Conference (NEWCAS)*, IEEE 10th International, 2012

[5] M. Suyama, Y.Kawai, S.Kimura, N.Asakura, K.Hirano, Y.Hasegawa, T.Saito, T.Morita, M.Muramatsu, K.Yamamoto, " A Compact Hybrid Photodetector (HPD)", *IEEE TRANSACTIONS ON NUCLEAR SCIENCE*, VOL. 44, NO. 3, JUNE 1997

[6] Sentaurus Reference Manual 2014,SYNOPSYS

[7] P. Cushman, R.Rusack, " A photomultiplier tube incorporating an avalanche photodiode", *Nuclear Instruments and Methods in Physics Research,* A333, pp. 381-390, 1993

[8] R. DeSalvo, W.Hao, K.You, Y.Wang, C.Xu, " First results on the hybrid photodiode tube", *Nuclear Instruments and Methods in Physics Research*, A315, pp.375-384, 1992

[9] Krzysztof Iniewski, *Semiconductor Radiation Detection System*, Taylor and Francis Group, LLC, 2010

[10] Tomer Lietner, Amos Feiningstein, Renato Turchetta, Rebecca Coath, Steven Chick, Gil Visokolov, Vitali Savuskan, Michael Javitt, Lior Gal, Igor Brouk, Sharon Bar-Lev, and Yael Nemirovsky, " Measurement and Simulation of Low Dark Count Rate Single Photon Avalanche Diode Device in a Low Voltage 180nm CMOS Image Sensor Technology", *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 60, NO. 6, JUNE 2013

[11] Justin A. Richardson, Eric A. G. Webster, Lindsay A. Grant, Robert K. Henderson, " Scalable Single-Photon Avalanche Diode Structures in Nanometer CMOS Technology", *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 58, NO. 7, JULY 2011

[12] L. Pancheri, David Stoppa, " Low-noise CMOS single-photon avalanche diodes with 32 ns dead time," *Proc. IEEE Eur. Solid-State Devices Conf.,* Munich, Germany, pp. 362–365, , Sep. 2007.

[13] Lin Qi, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon, Lis K. Nanver, " Low Dark-Count Pure B Single-Photon Avalanche Diode", *IEEE TRANSACTIONS ON ELECTRON DEVICES,* VOL. 61, NO. 11, NOVEMBER 2014

[14] Lin Qi, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon, Lis K. Nanver, " UV sensitive Low Dark-Count Pure B Single-Photon Avalanche Diode", *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 61, NO. 11, NOVEMBER 2014

[15] J.C. Ashley, C. J. Tungt, R. H. Ritchie, and V. E. Anderson, "Calculation Of mean free paths and stopping powers of low energy electrons (<10KeV) in solids using a statistical model", *IEEE Transactions on Nuclear Science*, Vot.NS-23, No.6, December 1976

[16] D. J. Roulston, N. D. Arora, and S. G. Chamberlain, "Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of n+-p Silicon Diodes," *IEEE Transactions on Electron Devices*, vol. ED-29, no. 2, pp. 284–291, 1982

[17] J. G. Fossum, "Computer-Aided Numerical Analysis of Silicon Solar Cells," *Solid-State Electronics*, vol. 19, no. 4, pp. 269–277, 1976

[18] J. G. Fossum, D. S. Lee, "A Physical Model for the Dependence of Carrier Lifetime on Doping Density in Non degenerate Silicon," *Solid-State Electronics*, vol. 25, no. 8, pp. 741–747, 1982

[19] J. G. Fossum, R.P. Mertens, D.S. Lee, J.F. Nijs, "Carrier Recombination and Lifetime in Highly Doped Silicon," *Solid-State Electronics*, vol. 26, no. 6, pp. 569–576, 1983

[20] A Schenk,"A Model for the field and temperature dependence of Shockley-Read-Hall Lifetimes in Silicon*" Solid-Store Electronics,* Vol. 35, No. 1 I, pp. 158˜-15%. 1992

[21] L. Huldt1, N. G. Nilsson1 and K. G. Svantesson1, "The temperature dependence of band-to-band Auger recombination in silicon", *Appl. Phys. Lett.* 35, 776 (1979)

[22] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon*," IEEE Transactions on Electron Devices*, Vol .ED-30, NO.7, July

[23] J. W. Slotboom, H. C. DE Graff, "Bandgap Narrowing in Silicon Bipolar Transistors" Bandgap Narrowing in Silicon Bipolar Transistors" *IEEE Transactions on Electron Devices*, vol. ED-30, no. 7, pp. 764–769, 1983

[24] R. Van Overstraeten, H. DE MAN, "Measurement of the Ionization Rates in Diffused Silicon p-n Junctions", *Solid-State Electronics,* Pergamon Press 1970. Vol. 13, pp. 583-608

[25] Y. Okuto ,C. R. Crowell, "Threshold Energy Effect on Avalanche Breakdown Voltage in Semiconductor Junctions", *Solid-State Electronics*, ,V ol1.8 p,p.1 61468P, 1975

[26] Thomas Lackner, "Avalanche Multiplication in Semiconductors: A Modification Of Chtnoweth's Law", *Solid-State Electronics*, Vol. 34, No. 1, pp. 33-42, 1991

[27] James D. Plummer, Michael Deal, and Peter B. Griffin,"*Silicon VLSI Technology: Fundamentals, Practice and Modeling*", *1*st ed, Pearson Education India, 2009

[28] Ashok Kumar Ray,"Plasma Immersion Ion Implantation Process Space Optimization for Semiconductor Device Applications", *A dissertation submitted in partial fulfillment of the requirements for the degree of Master of Technology IIT Bombay*, June 25 2012

[29] SHU QIN, James D Bernstein and Chung Chan ,"Hydrogen etching for semiconductor materials in plasma doping experiments", *Journal of Electronic Materials*, Vol 25, No.3, 1996

List of Publications

[1] Harsha S, Kaushik Nayak, Shiv Govind Singh, "Simulation and Fabrication of Silicon Avalanche Diode as a Multiplier in Hybrid Photo Detector", *IEEE Sensors*, 2016 (Under Review)