An Enhanced Recycling Folded Cascode OTA with a Positive Feedback

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Abstract- In this paper an enhanced fully differential recycling folded cascode operational trans conductance amplifier that achieves higher DC gain with same power and area as that of recycling folded cascode OTA is discussed. Generally, the output impedance of the cascode amplifier depends on the current flowing into the cascode node. Hence, in order to increase the DC gain of the conventional Recycling Folded Cascode OTA the modification is done at the cascode node. The proposed enhanced fully differential RFC OTA is implemented in strong inversion using gm/Id methodology. The design is carried out using UMC180nm technology and studied through simulation. From simulation, we found an increase in DC gain of 9dB, 14dB, and 24dB is achieved without changing the Unity Gain Bandwidth.

I. INTRODUCTION

High performance A/D converters and switched capacitor filters requires Operational Trans conductance Amplifiers (OTA) that have both high DC gain and a high unity gain bandwidth (UGB). The advent of deep sub-micron technologies enable increasingly high speed circuits, but designing of high DC gain OTAs is more difficult due to the decrease of intrinsic gain $g_m r_o$ of the transistor. One of the most commonly used architectures, as a single stage or first stage in multi stage amplifiers had been the Folded Cascode (FC) amplifier for its high gain and reasonably large output signal swing in low voltage CMOS process. Moreover the PMOS input FC has become the prime choice over its NMOS counterpart for its higher non-dominant poles, lower flicker noise, and input common mode level [1].

In [3], [4] an enhanced fully differential folded cascode op amp is proposed. The enhancement consists of additional current path at the cascode node which is used to convert the current sources into active current mirrors – allowing the output current to increase above its quiescent value during slewing. In [2], the bias current sources of the conventional FC which consume more current that doesn't contribute to DC gain. This disadvantage is overcome in Recycling Folded Cascode (RFC) by utilizing the current recycling technique in which the bias current sources contributes to the enhancement of the DC gain of the OTA without affecting the output impedance. In this paper a positive feedback technique is proposed which increases the dc gain and has added advantage of decreasing the common mode gain of RFC.

The paper is organized as follows. Section II briefs about the conventional RFC OTA. Section III discusses the problem at the cascode node of the cascode amplifiers. Section IV discusses about the proposed solution for Cascode amplifier. Section V discusses about the proposed Enhanced RFC OTA (ERFC), Section VI describes CMRR

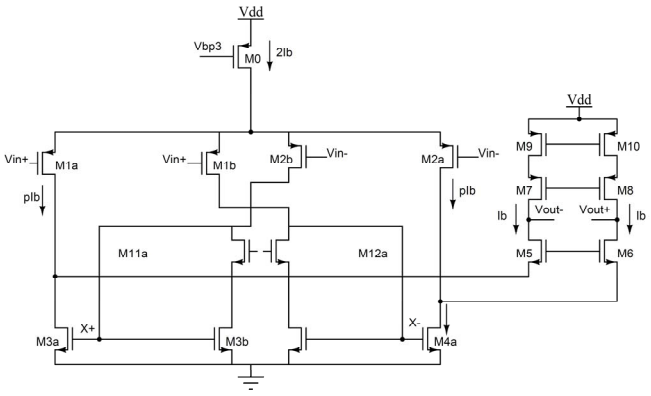

Fig1. Recycling Folded Cascode OTA

of ERFC. Section VII briefs about the simulation results. Section VIII about the conclusion.

II. RECYCLING FOLDED CASCODE OTA

The bias current source in the conventional FC [1] consumes more current, and has the largest trans conductance. However, these current sources don't contribute to the DC gain. In [2], the input transistors of FC are split into two parts (M1a, M1b, M2a, M2b) which conducts fixed and equal currents. Next the current source transistor in the FC is replaced by current mirrors M3a:M3b and M4a:M4b at a ratio of K: 1.This architecture is called as the RFC OTA which is shown in Fig.1.

A. DC Gain

The DC gain A_v of the RFC [2] is given by

$$A_v = G_m * R_{OUT} \quad (1)$$

Where G_m is the trans conductance and R_{OUT} is the output impedance.

The trans conductance Gm is given by (2).

$$G_m = I_{OUT}/V_{i+} \quad (2)$$

Where the output current I_{OUT} is given by (3)

$$I_{OUT} \approx g_{m1a}V_{i+} + g_{m3a}V_{x+} \quad (3)$$

From Fig.1 it can be seen that transistors M2b, and the diode connected transistors M11 and M3b acts as a common source amplifier with a voltage gain of approximately -1. Since, the input applied to M2b is in opposite direction, the node X_+ (or X_-) is in the same phase of V_{i+} (or V_{i-})

Where $V_{x+} \approx -g_{m2b}R_X V_{i-}$ and $R_X = 1/gm3b$

Hence $V_{x+} \approx V_{i+}$

Substituting V_{x+} in (3)

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$$I_{OUT} \approx g_{m1a}V_{i+} + g_{m3a}V_{i+} \quad (4)$$

Substituting (4) in (2) gives the small signal trans conductance G_m.

$$Gm = g_{m1a} + g_{m3a} \quad (5)$$

Where $g_{m3a} \approx K.\ g_{m1a}$

The output impedance R_{OUT} of the RFC OTA is given by (6)

$$R_{OUT} \approx g_{m5}r_{o5}(r_{o1a}||r_{o3a})||g_{m7}r_{o7}r_{o9} \quad (6)$$

Sub (5) and (6) in (1), the A_V is given by (7)

$$A_V \approx gm1a(K+1).\ g_{m5}r_{o5}(r_{o1a}||r_{o3a})||g_{m7}r_{o7}r_{o9} \quad (7)$$

B. Frequency Response Analysis:

From Fig.1 it is observed that there are three poles and one zero. For simplicity we consider only the poles occurring at the output node and cascode node.

1. Dominant Pole: Because of high impedance of the circuit (R_{OUT}) and large capacitance (C_{OUT}) is seen at the output node the dominant pole occurs in this node.

The dominant pole frequency wp1 is given by

$$Wp1 \approx 1/R_{OUT}.\ C_{OUT} \quad (8)$$

Where

$$R_{OUT} \approx g_{m5}r_{o5}(r_{o1a}||r_{o3a}) \,||\, g_{m7}r_{o7}r_{o9}$$

and

$$C_{OUT} \approx C_L+C_{DB8}+C_{GD8}+C_{GD6}+C_{DB6}$$

2. Non-Dominant Pole: It occurs in the cascode node with a frequency much greater than the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance R_C at the cascode node is approximately 1/gm5. Hence the non-dominant pole frequency is given by

$$Wp2 \approx 1/R_C.C_C \quad (9)$$

Where $C_C \approx C_{GD3a}+C_{GS5}+C_{GD1a}+C_{DB3a}+C_{DB1a}+C_{SB5}$

The UGB of the OTA is given by (10)

$$UGB \approx gm1a(K+1)/C_{OUT} \quad (10)$$

From (7) and (10) it is observed that the A_V and UGB is enhanced by a factor of (K+1) compared to the FC for the same power.

III. PROBLEM AT THE CASCODE NODE

In Fig.2 the input generated trans conductance current ($i_{in} = g_m vin$) of the input transistor M1 is resistively divided at the cascode node c between two competing current paths formed by r_{o1} of the input transistor M1 and the impedance looking into the source of cascode transistor M2 which is given by Z_C. If the output load of the cascode amplifier is very high, the impedance seen at the input of the cascode node is given by (11)

$$Z_c = \frac{1}{g_{m2}}\left(1 + \frac{R_{load}}{r_{02}}\right) \cong \frac{R_{load}}{g_{m2}r_{02}} \quad (11)$$

From (11) it is observed that the input impedance is on the order of output impedance. As a result i_{in} is distributed approximately equal to r_{o1} and Z_C allowing ½ of i_{in} to generate V_{OUT}. This empirically observed DC gain of the cascode amplifiers being typically less than the theoretical $(g_m r_0)^2$. [3]

In [4] it is seen that the output impedance can be increased by decreasing the input impedance at the cascode node or by increasing the r_{01}.In order to increase the input impedance i.e Z_{c1} at the cascode node a voltage-based positive feedback technique is adopted and discussed in next section.

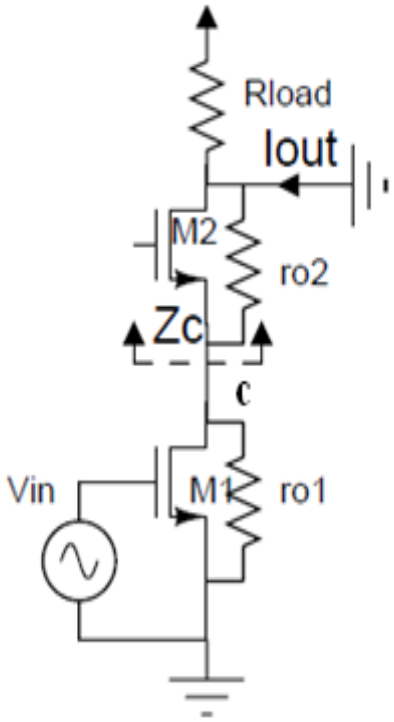

Fig.2.Cascode amplifier

IV. SOLUTION TO THE PROBLEM AT THE CASCODE NODE

In the cascode amplifier M2 acts as a common gate stage which amplifies a current signal given at the source of the M2 transistor. The current source given at the source of the M2 transistor should have very high impedance which is limited to r_0. This can be increased by using a positive feedback at the cascode node which introduces a negative resistance in parallel with the current source resistance similar to r_0 which increases the output impedance of the current source to almost infinity. This positive feedback at the cascode node is implemented by the use of two back to back inverters connected in cascade fashion shown in fig.2. The output impedance at the cascode node Vc is found to be

$$R_c = \frac{r_0}{(3-(gmro)^2)} \quad (12)$$

$$R_{out} = g_m r_0 R_c$$

To make the output impedance to be infinity the denominator of (12) should be zero. The maximum value of $g_m r_0$ of each inverter should be less than equal to 1.732 found from the denominator of the output resistance. If R_c exceeds this value then a right half plane pole will come into effect which makes the system unstable.

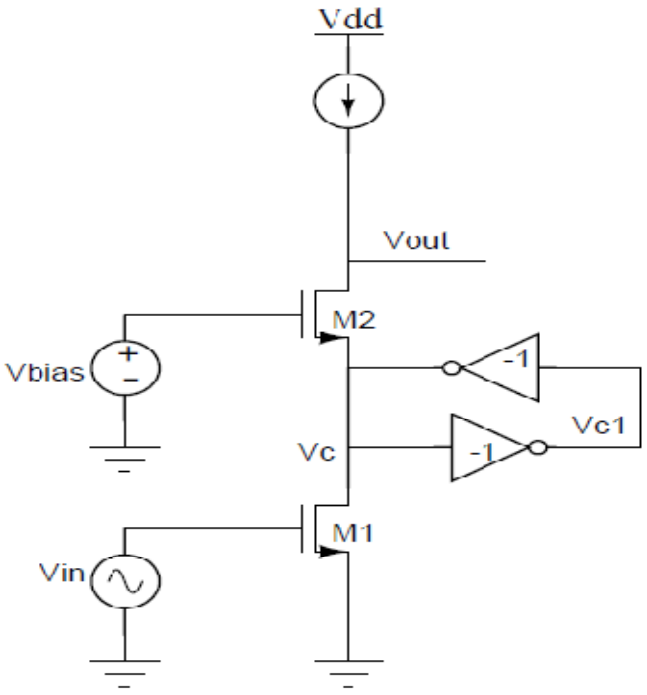

Fig.3. NMOS type Cascode amplifier with positive feedback

V. ENHANCED RFC OTA

In the previous section we have investigated that the positive feedback results increase in area and power by putting two inverters. This can be eliminated in RFC. To implement the positive feedback at Vc+ in Fig.4, we can take signal from the other cascode node Vc- and pass it through an inverter and the inverter output is given to Vc+ node. Similarly the same method can be implemented for Vc- cascode node. The inverters can be replaced by transistors M1c and M2c given in Fig.6. To implement in same area and same power we divide the M1b into two parts M1b and M1c in a ratio of a: b such that power consumption is constant to implement unity gain feedback at the gate of M3a we have to scale the width of M1b, M12, and M4b by 'a' compared to the RFC. To get the impedance at the cascode node Vc+ the input is grounded and the impedance at the cascode node is given by (13)

$$R_c \approx \frac{r_{01a}||r_{03a}||r_{02c}}{1-g_{m2c}(r_{01a}||r_{03a}||r_{02c})} \quad (13)$$

The cascode node impedance can be increased by decreasing the denominator (13) and the $g_{m2c}(r_{01a}||r_{03a}||r_{02c})$ should be less than equal to 1. If it exceeds beyond 1 then it introduces a right half plane pole which makes the system unstable so this condition should be fulfilled for proper operation of the circuit. The gain is also increased due to the increase in output impedance i.e.

$$R_{out} = (g_{m5} r_{05} R_c)||(g_{m7} r_{o7} r_{09})$$

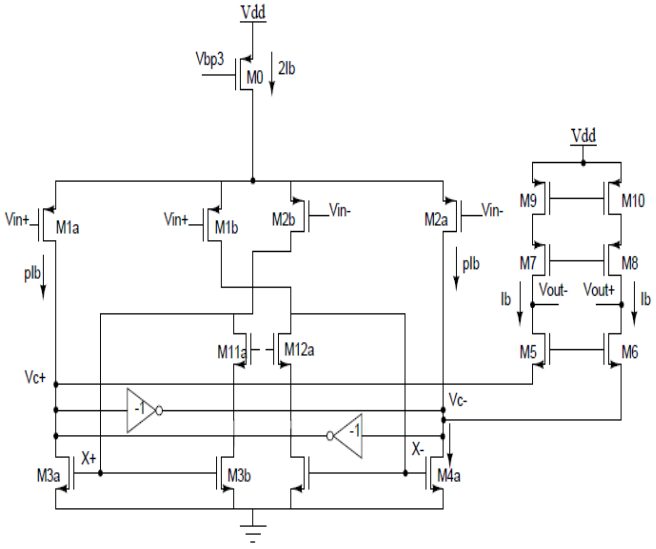

Fig.4. PMOS type RFC amplifier with positive feedback

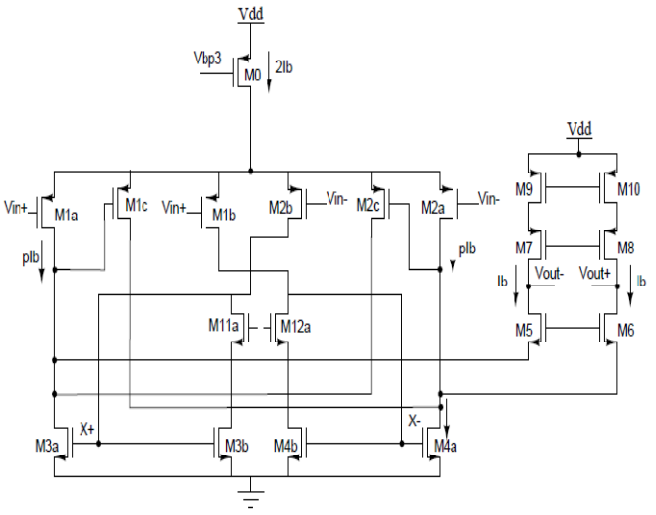

Fig.5. PMOS type RFC amplifier with positive feedback

The signal at the cascode node can be improved by the positive feedback operation of the inverters. The swing of the signal at the cascode node is increased by the positive feedback operation of the inverters as the signals are added in the same phase at the cascode node.

Frequency Response Analysis

1. Dominant Pole: Because of high impedance of the circuit (R_{OUT}) and large capacitance (C_{OUT}) is seen at the output node the dominant pole occurs in this node.

The dominant pole frequency ω_{p1} is given by

$$\omega_{p1} = \frac{1}{R_{out} C_{out}} \quad (14)$$

Where

$$R_{out} = (g_{m5} r_{05} R_c)||(g_{m7} r_{o7} r_{09})$$

And

$$C_{out} = C_L + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

If $g_{m2c}(r_{01a}||r_{03a}||r_{02c}) \gg 1$, then

$$R_c \cong \frac{-1}{g_{m2c}}$$

If $g_{m2c} \approx g_{m5}$

$$R_{out} \cong (-r_{05})||(g_{m7}r_{07}r_{09}) \approx -r_{05}$$

And

$$C_{out} = C_L + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

$$\omega_{punstable} = \frac{1}{R_{out}C_{out}} \quad (15)$$

After $\omega_{punstable}$the phase margin starts increasing due to the right hand pole and the gain starts decreasing at 20dB per decade. It becomes unstable as the time domain response increases exponentially without settling to a maximum voltage. The gain decreases because of decreasing of the output resistance i.e. -r_{05}. The gain equation becomes

$$A_v = G_{munstable} * R_{outunstable}$$

$$G_{munstable} = g_{m1a} * (1 + K)$$

$$R_{outunstable} = -r_{05}$$

As the output resistance is very less so the right hand pole will be generated at a higher frequency compared to that of stable operation.

2. Non-Dominant Pole: It occurs in the cascode node with a frequency much greater than the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance R_C at the cascode node is approximately 1/gm5. Hence the non-dominant pole frequency is given by

$$\omega_{p2} \approx \frac{1}{R_c C_C}$$

Where

$$C_c \approx C_{GD3a} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5} + C_{gs1c} + C_{gs3c}$$

As the current is flowing in $M_{3a}$is more compared to the previous design so the capacitance value C_{DB3a} is increased due to the increase in the width of the M_{3a}. The UGB of the OTA is given by (16) .

$$UGB \approx g_{m1a}(K+1)/C_{OUT} \quad (16)$$

From (16) it is observed that the UGB of the ERFC OTA remains same as that of the RFC OTA. As the M1c and M3c are added to the cascode node the parasitic capacitance at the cascode node will increase and it will degrade the phase margin. As the resistance is directly proportional to the trans conductance so to improve the resistance the trans conductance should be increased and the trans conductance can be improved by only passing more current or increasing the width of M1c which leads to increase in the width of M1c and the parasitic capacitance at the cascode node will increase decreasing the phase margin. To increase the phase margin we can decrease the dc current flowing through M1c such that the capacitance effect at the cascode node is less. To show the variation in gain and phase margin three OTAs with different values of g_{m1c} are simulated and the characteristics are observed. The gain increases as the trans conductance of M1c increases which proves the output resistance increases with increase in current through M1c transistor.

VI. COMMON MODE REJECTION RATIO

The difficulties posed by common -mode operation of differential circuits have been proposed in numerous papers i.e. (5), (6). In most differential amplifiers, the common mode and differential-mode signals share the same signal path, resulting in equal and large common mode and differential mode impedance. The difference between the common-mode and differential–mode gain is just the difference between g_{m1} and the output conductance of its tail current source. In the enhanced op-amp topology, the high output resistance which leads to high differential output gain does not occur for common mode signals as the positive feedback acts as a negative feedback for common mode signals and the signals are subtracted in the cascode node and the common mode gain is given by product of (17) and (18)

$$g_{mERFC} = g_{m1a}(K - 1) \quad (17)$$

$$R_c \approx \frac{r_{01a}||r_{03a}||r_{02c}}{1 + g_{m2c}(r_{01a}||r_{03a}||r_{02c})} \quad (18)$$

VII. SIMULATION RESULTS

To validate the theoretical results presented thus far, a Recycling Folded Cascode OTA is designed as a benchmark following proven analog design practices: The RFC OTA proposed in the literature [2] and Enhanced RFC OTA proposed in this paper are designed in the strong inversion region. They are simulated using UMC180nm CMOS process with a supply voltage of 1.8 Volts. M1b in RFC OTA is split into M1c and M1b in ERFC OTA for three different current ratios. (One third, One half and Two Third). The transistor sizes are determined by using g_m/I_D methodology [7] for three current ratios (a:b) of (2/3:1/3), (1/2:1/2) and (1/3:2/3) . From Fig.9 and Fig.10, it is observed that in strong inversion region, for the three current ratios, the DC gain increases by 9dB, 13dB and 24dB respectively and CMRR increases by 15dB, 20dB and 30dB respectively. The slew rate increases by 1.12 for all the current ratios as shown in Fig.11.

VIII. CONCLUSION

The enhanced RFC OTA proposed in this paper and RFC OTA reported in the literature have been designed and simulated in UMC 180nm CMOS technology in strong inversion. The increase in the low frequency DC gain is achieved by positive feedback technique. This in turn results in high slew rate and high

common mode rejection ratio. The differential Enhanced RFC OTA achieves a higher DC Gain and lower common mode gain compared to the RFC OTA.

REFERENCES

[1] Behzad Razavi, "Design of **A**nalog CMOS Integrated Circuit Tata McGraw" Hill 2001.

[2] Rida.S.Assaad and Jose Silva-Martinez, "The Recycling folded cascode: A general enhancement of the folded cascode amplifier" IEEE Journal of Solid State Circuits, Vol.44, No.9, September 2009.

[3] K.Nakamura and L.R. Carley, "An enhanced fully differential folded cascode op-amp" IEEE Journal of Solid-State Circuits, vol.27.pp.563-568, APR.1992.

[4] L. Richard Carley, Katsufumi Nakamura, "Fully differential operational amplifier having frequency dependent impedance division" Patent Number 5,146,179.

[5] R.T. Kaneshiro, "Circuit and Technology considerations for high frequency switched capacitor filters" Ph.D. dissertation, Univ.Calif, Berkeley July 1983

[6] D.Sendrowicz, S.F.Dreyer, J.H. Huggins, C.F. Rahim, and C.A.Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip" IEEE J. Solid-State circuits, vol.SC-17,no.6, pp.1014-1023, Dec.1982

[7] David M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design", A John Wiley and Sons, Ltd., Publication 2009.

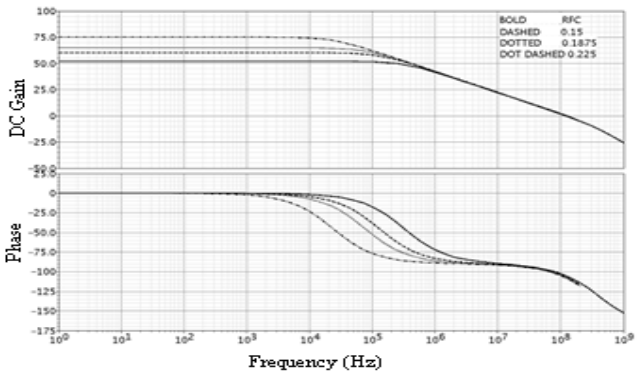

Fig.6. Gain and Phase plots of RFC and ERFC

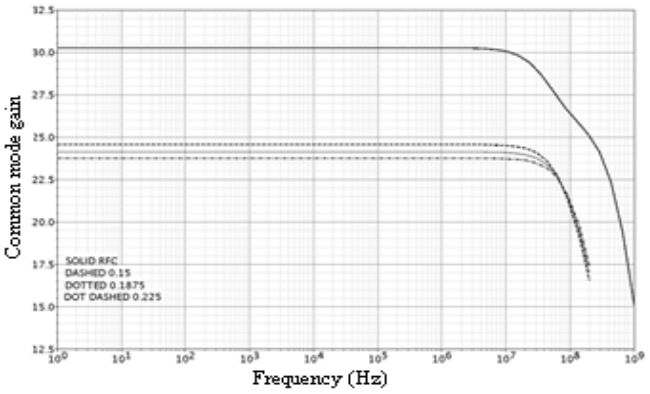

Fig.7. Common Mode Gain plots of RFC and ERFC

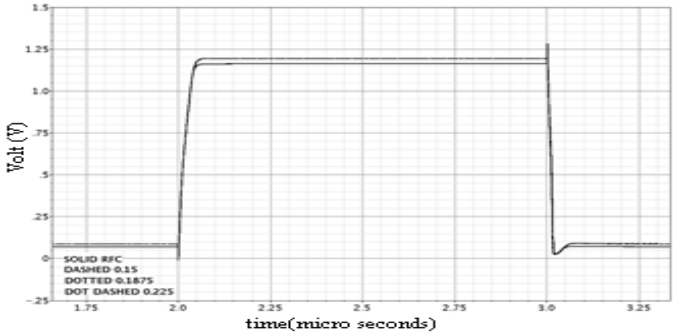

Fig.8. Slew Rate of RFC and ERFC

Table.1. Comparison of RFC and Proposed ERFC OTA

Design parameters	RFC	ERFC OTA with current ratio (a:b) Of		
		2/3:1/3	1/2:1/2	1/3:2/3
Current Consumption (μW)	560	560	560	560
DC (Open loop Gain) (dB)	51	60	65	75
Unity gain Bandwidth (MHz)	120	120	120	120
Phase Margin(deg)	75	73	73	72
CMRR(dB)	21	35	40	52
Slew Rate ($V/\mu s$)	49	55	55	55
FOM (((V/µs)pF)/mA)	686	770	770	770